

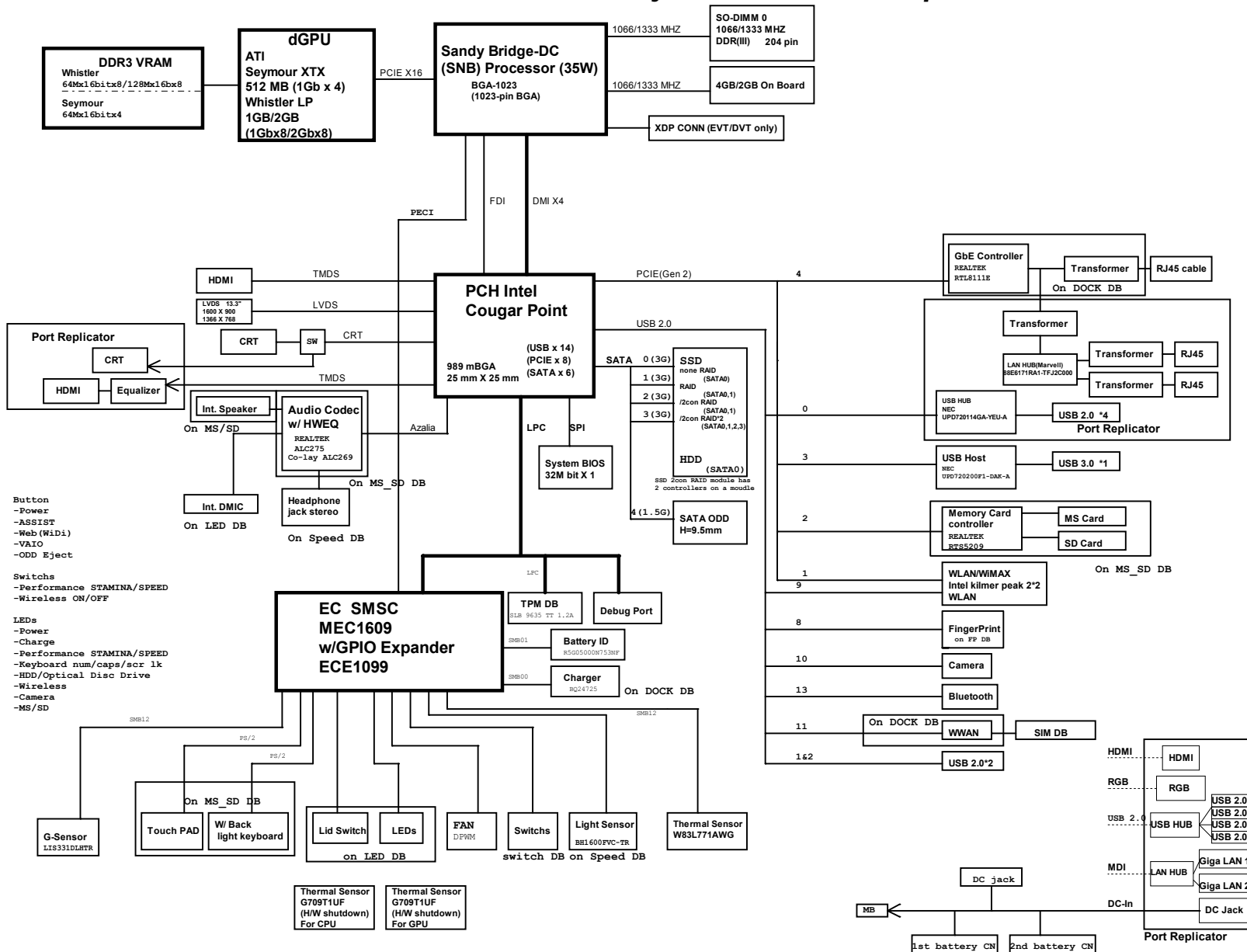
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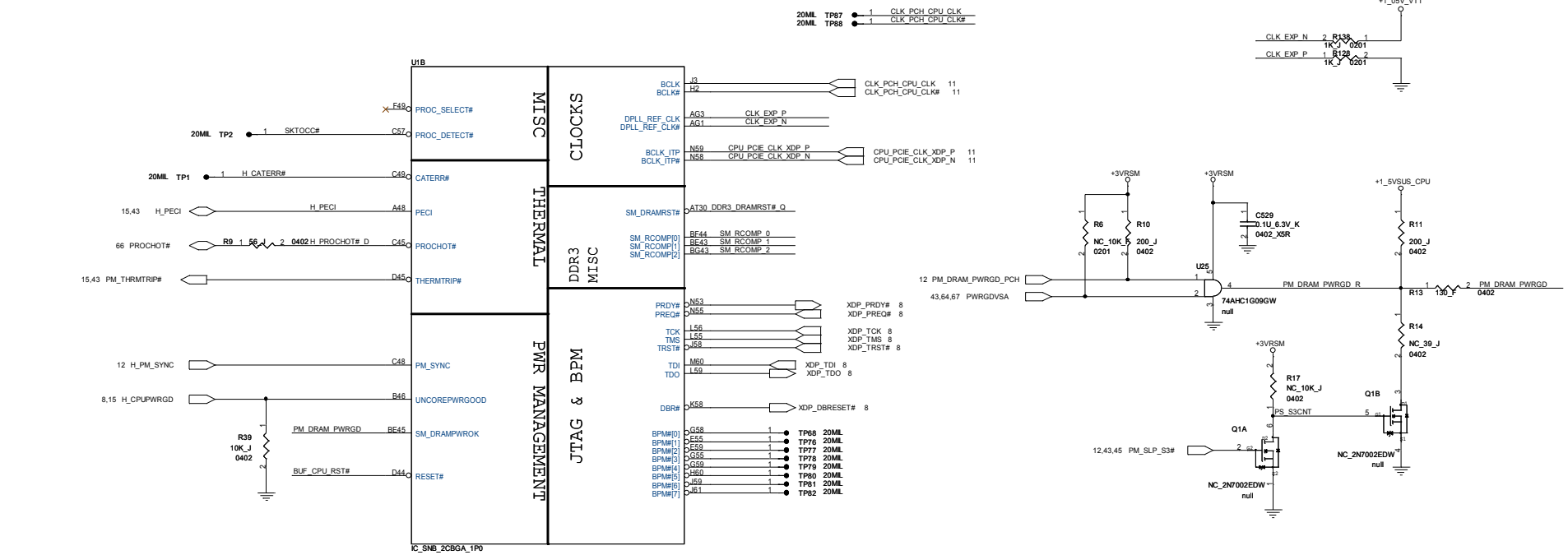
Project Code & Schematics Subject:	PCB P/N:
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P. Leader	Check by	Design by

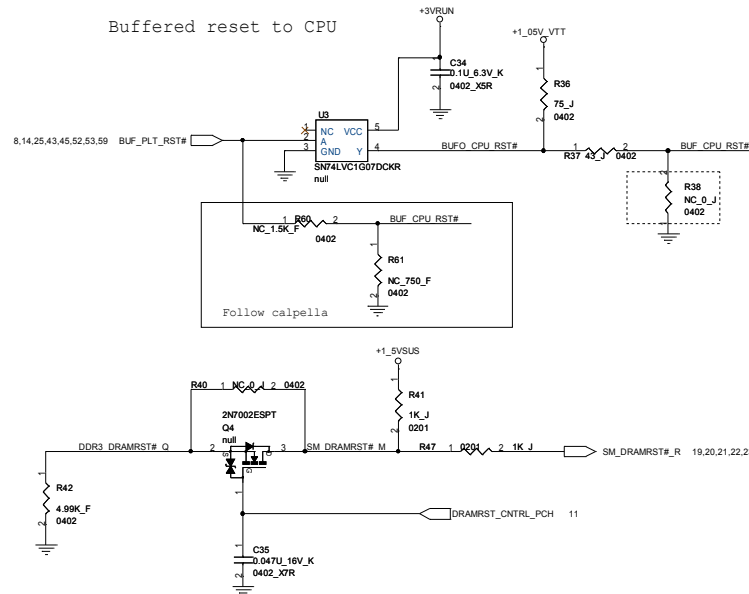
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	Index Page		
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Huron River Platform+ ATI Whistler/Seymour Discrete Graphic

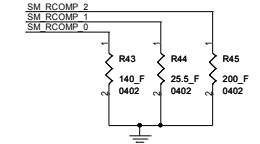




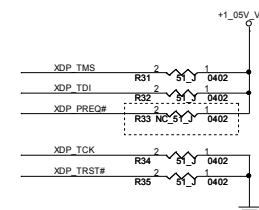
Buffered reset to CPU

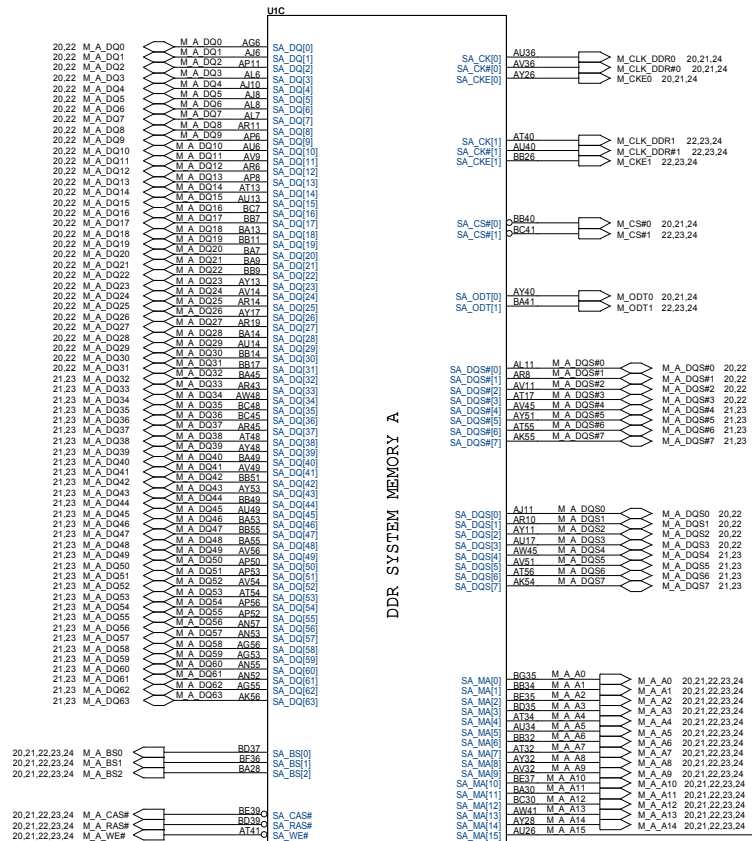


DDR3 Compensation Signals

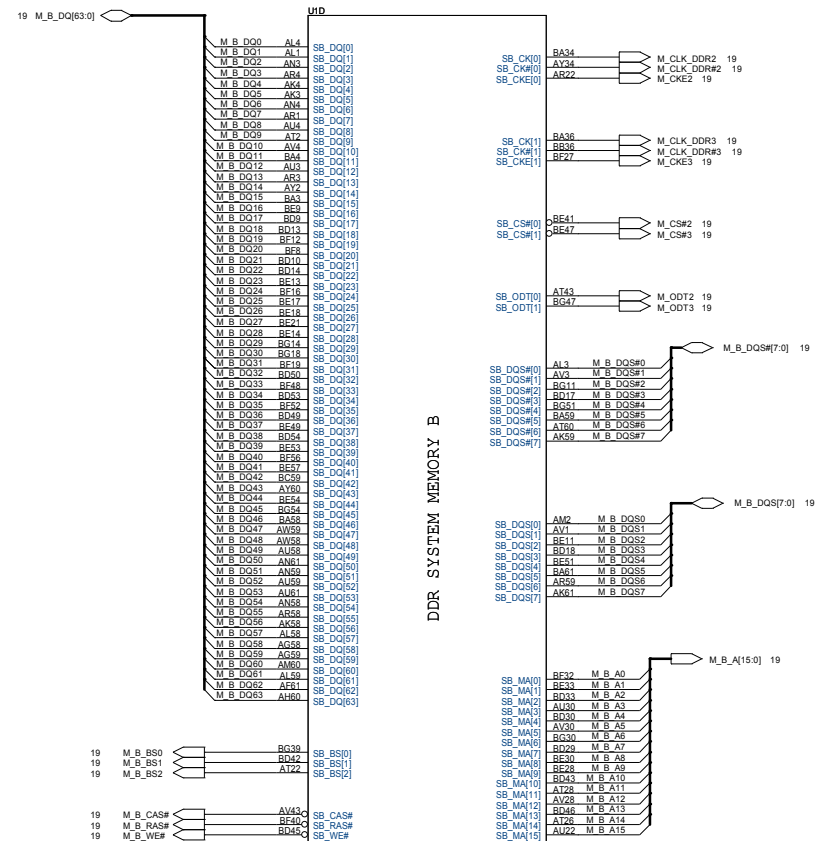


PU/PD for JTAG signals



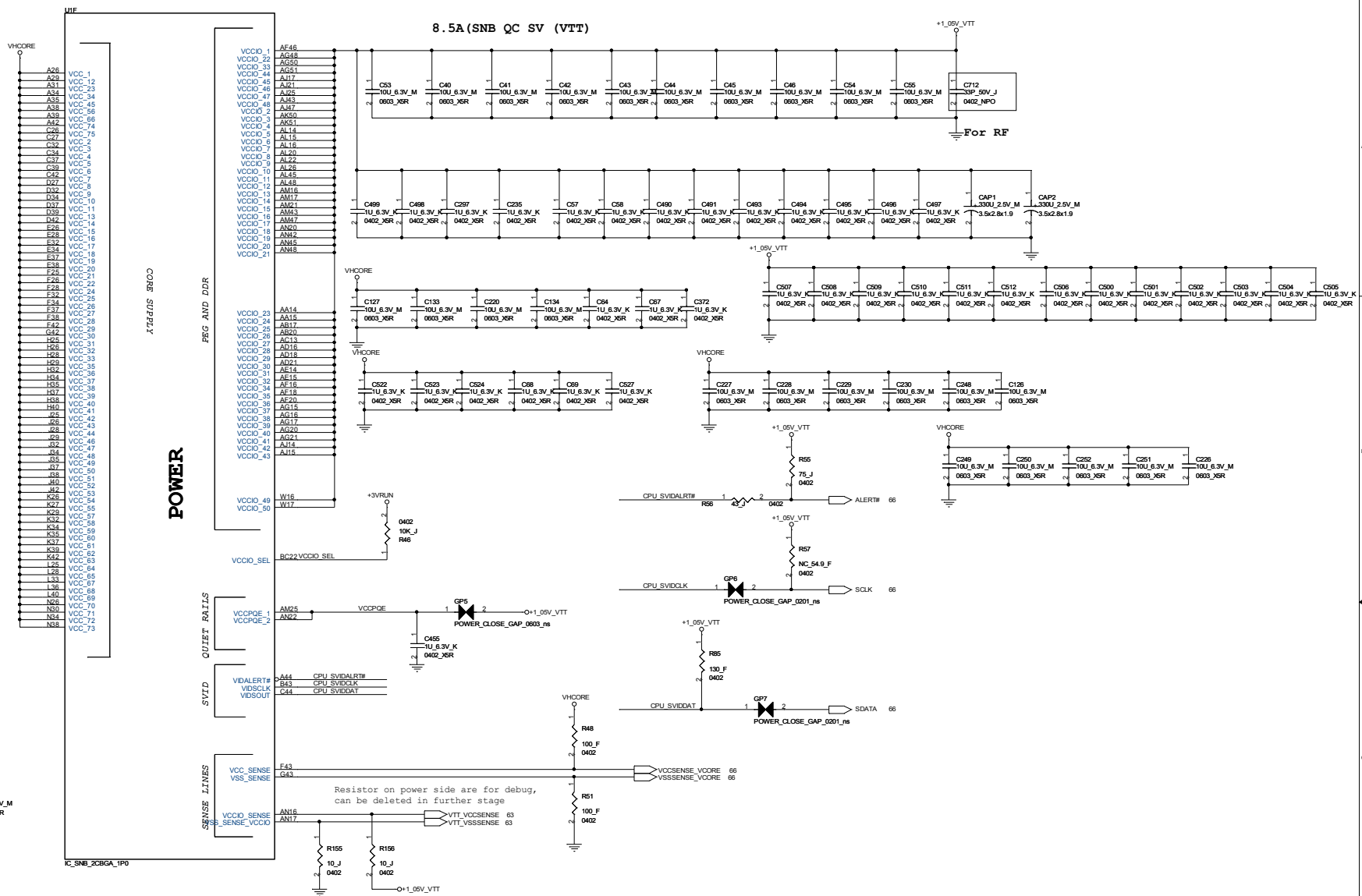
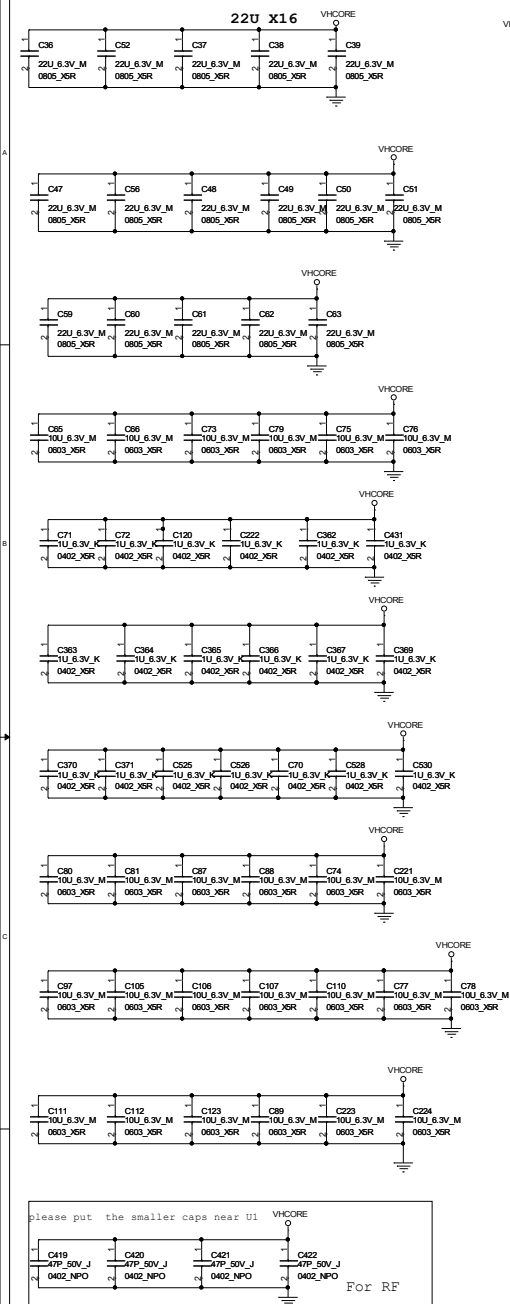


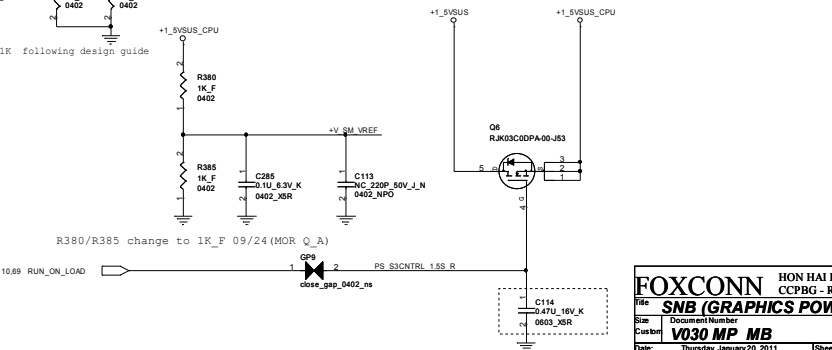
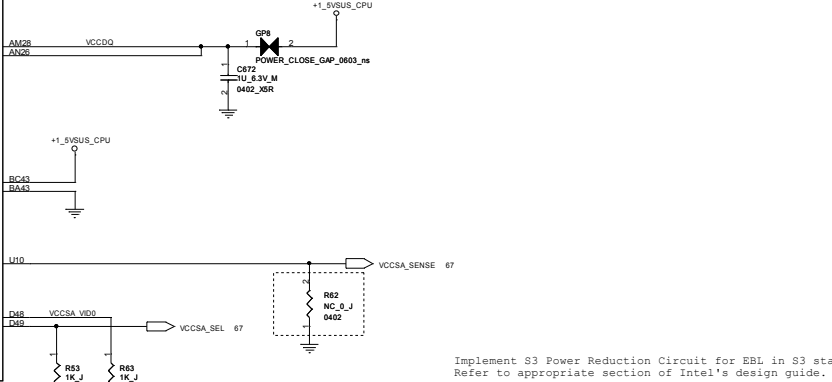
IC_SNB_2CBGA_1P0

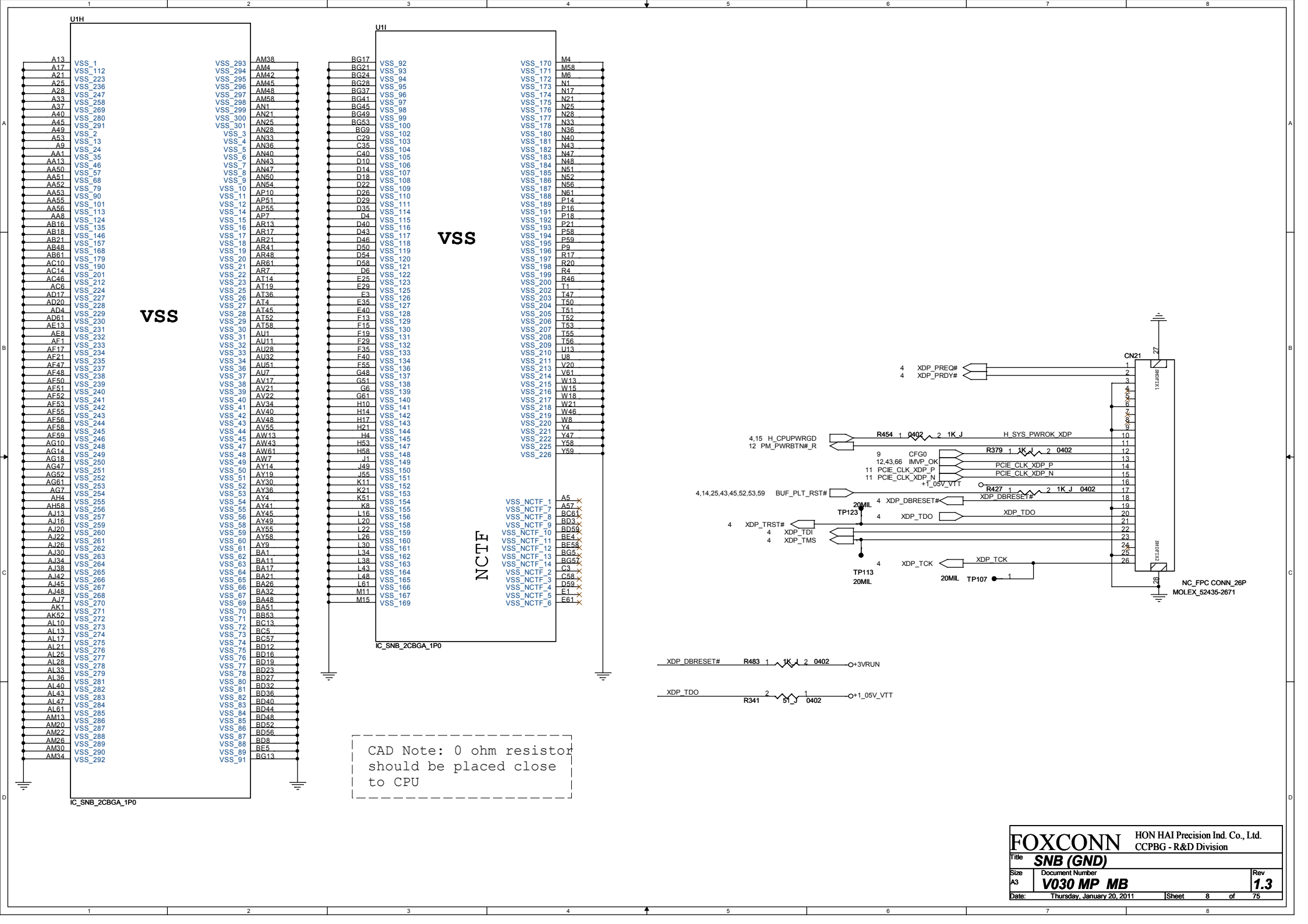


IC_SNB_2CBGA_1P0

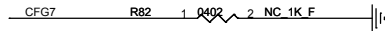
53A (SNB QC SV)





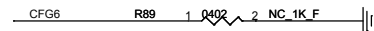
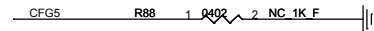


PEG static Lane Reversal - CFG2 is for 16X		
CFG2	0	LANE Reversed
	1	(Default)Normal Operation

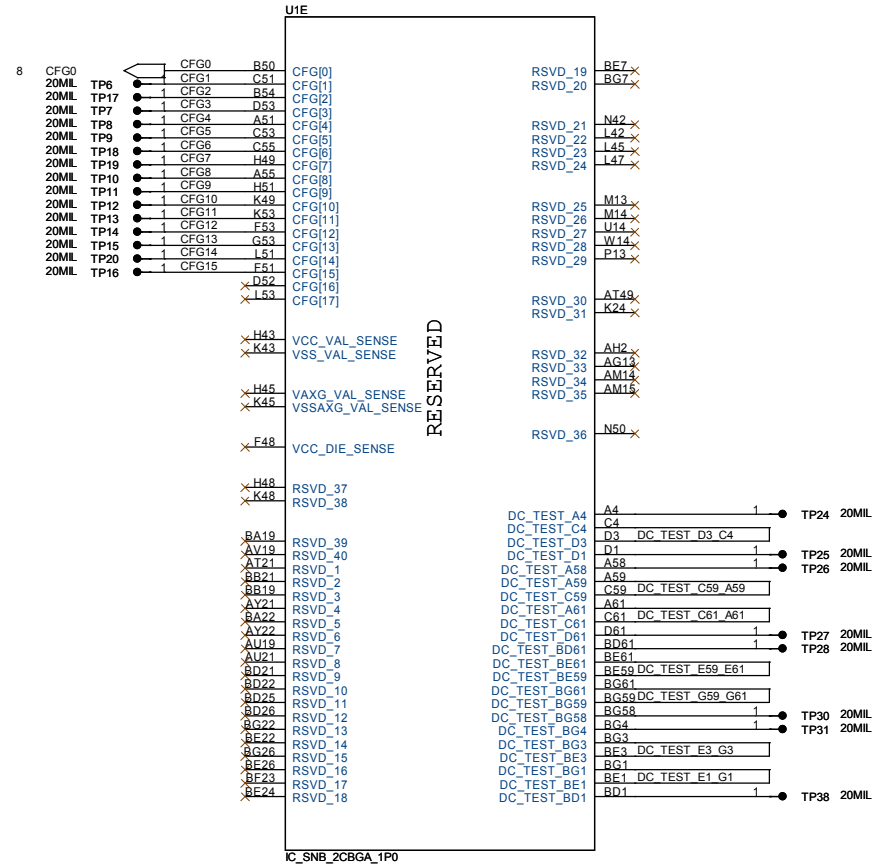


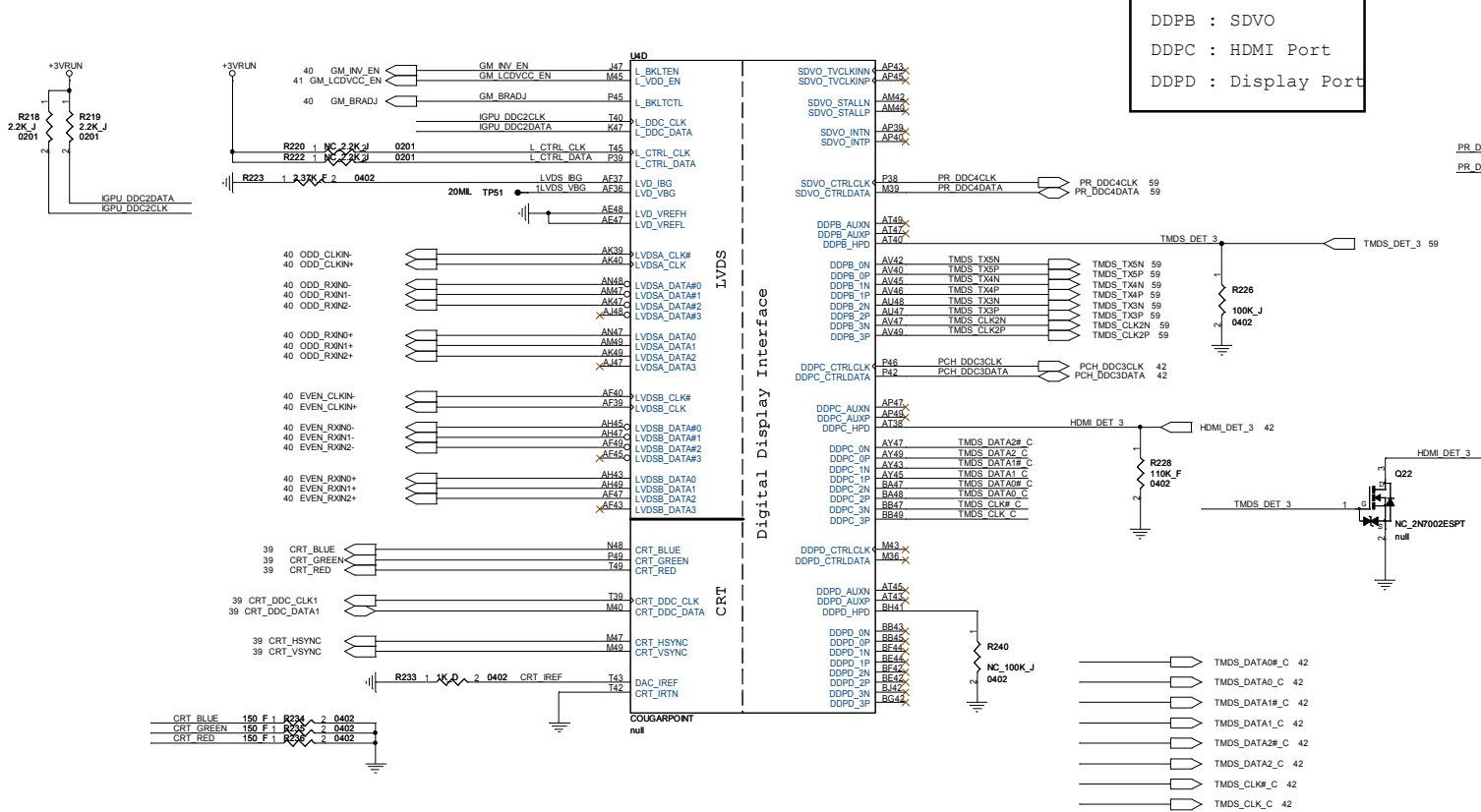
PEG DFER Training		
CFG7	0	PEG Wait for Bios for Training
	1	(Default)PEG Train immediately following xxResetB Deassertion

Display Port Presence Strap		
CFG4	0	(Default) Enabled
	1	Disabled



Display Port Presence Strap		
CFG[6:5]	11	(Default)16X
	10	X8 X8
	01	Reserved
	00	X8 X4 X4

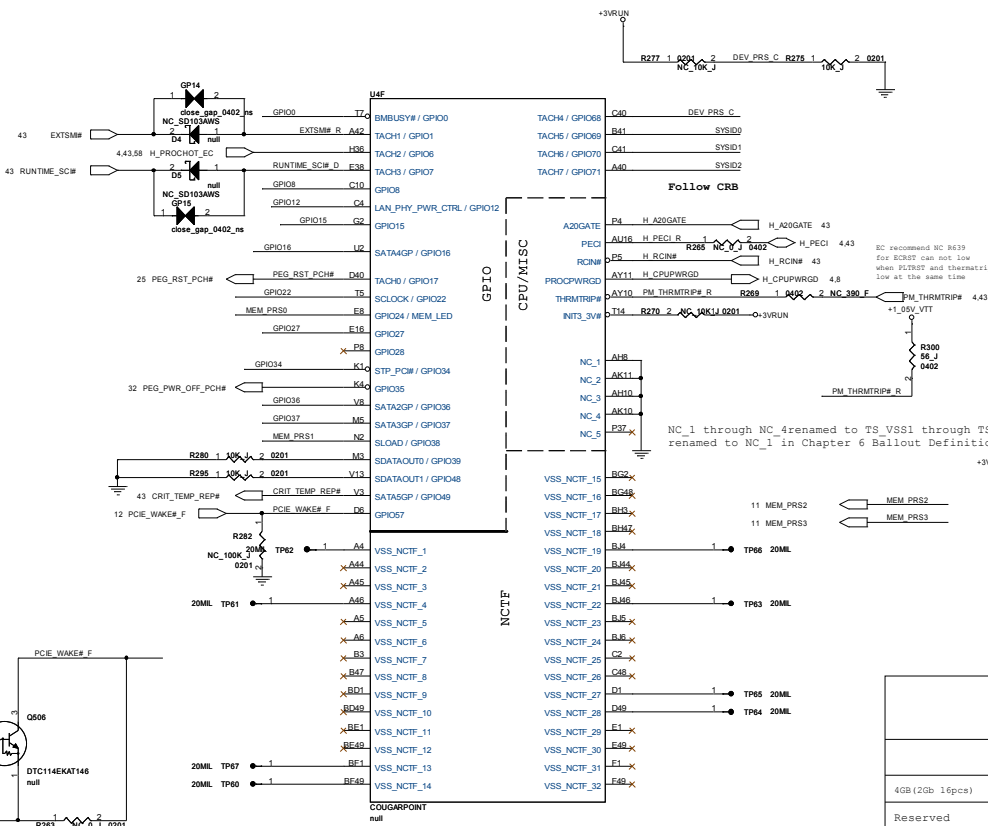
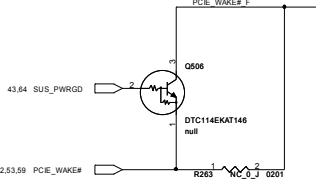
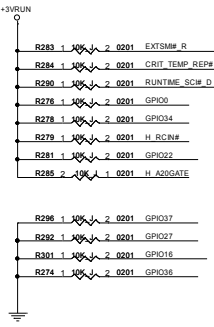
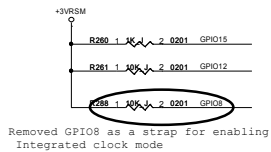




	DEV_PRS_A	DEV_PRS_B
Mild	L	L
Mild-B	L	H
Hot	H	L
Reserved	H	H

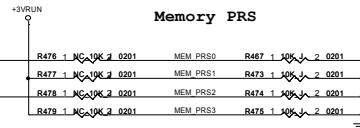
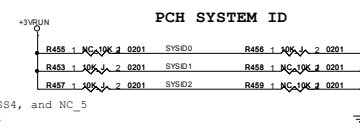
PM_EXTTIS#0	PM_EXTTIS#1	Threshold
0	0	HOT
1	0	HOT
0	1	WARM
1	1	OFF

USB PORT	Function
PORT-0	PR USB2.0 port
PORT-1	USB 2.0
PORT-2	USB 2.0
PORT-3	
PORT-4	
PORT-5	
PORT-6	
PORT-7	
PORT-8	Fingerprint
PORT-9	Wireless LAN (WiMAX)
PORT-10	Camera
PORT-11	WAN
PORT-12	
PORT-13	Bluetooth

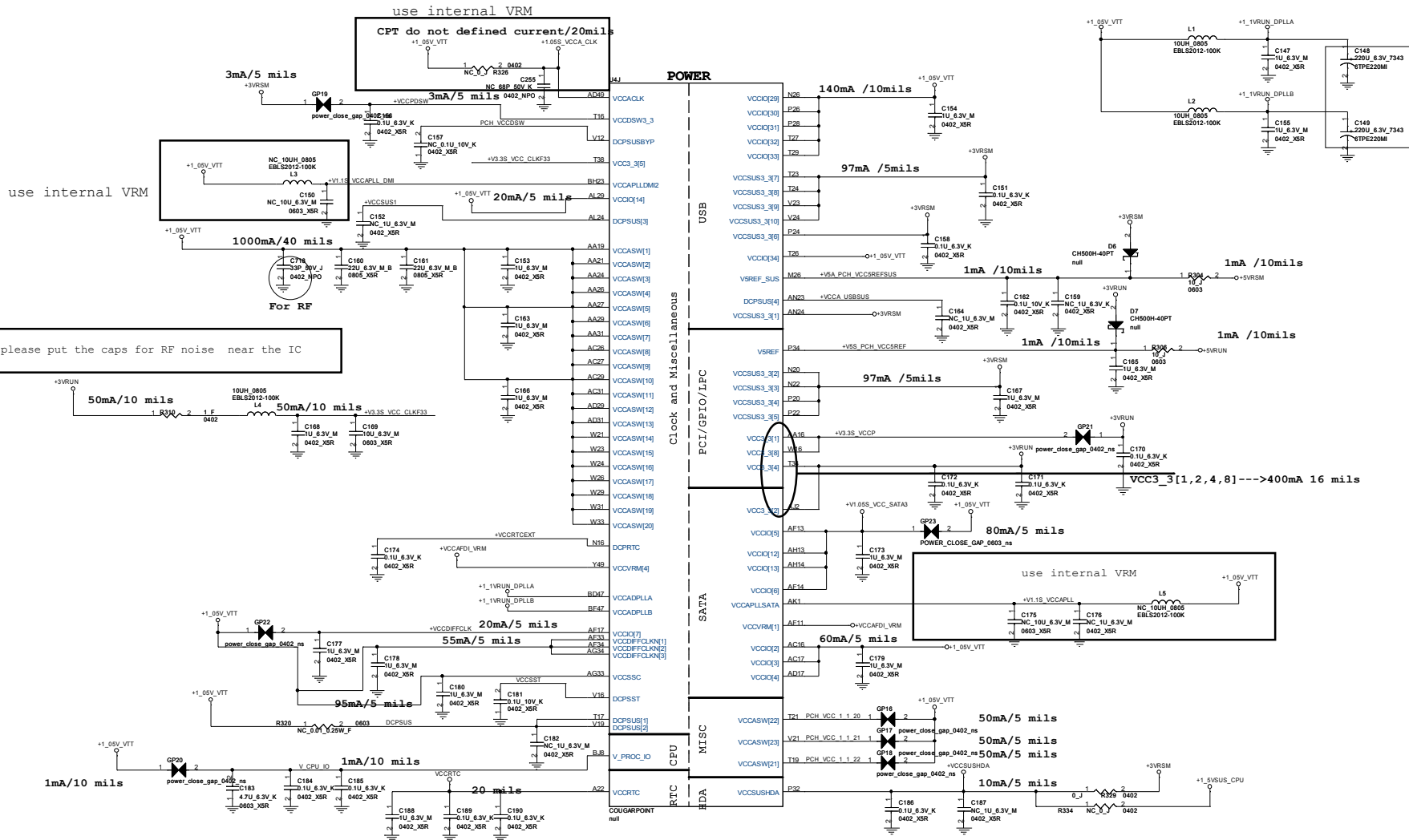


	DEV_PRS_C
13''	L
15''	H

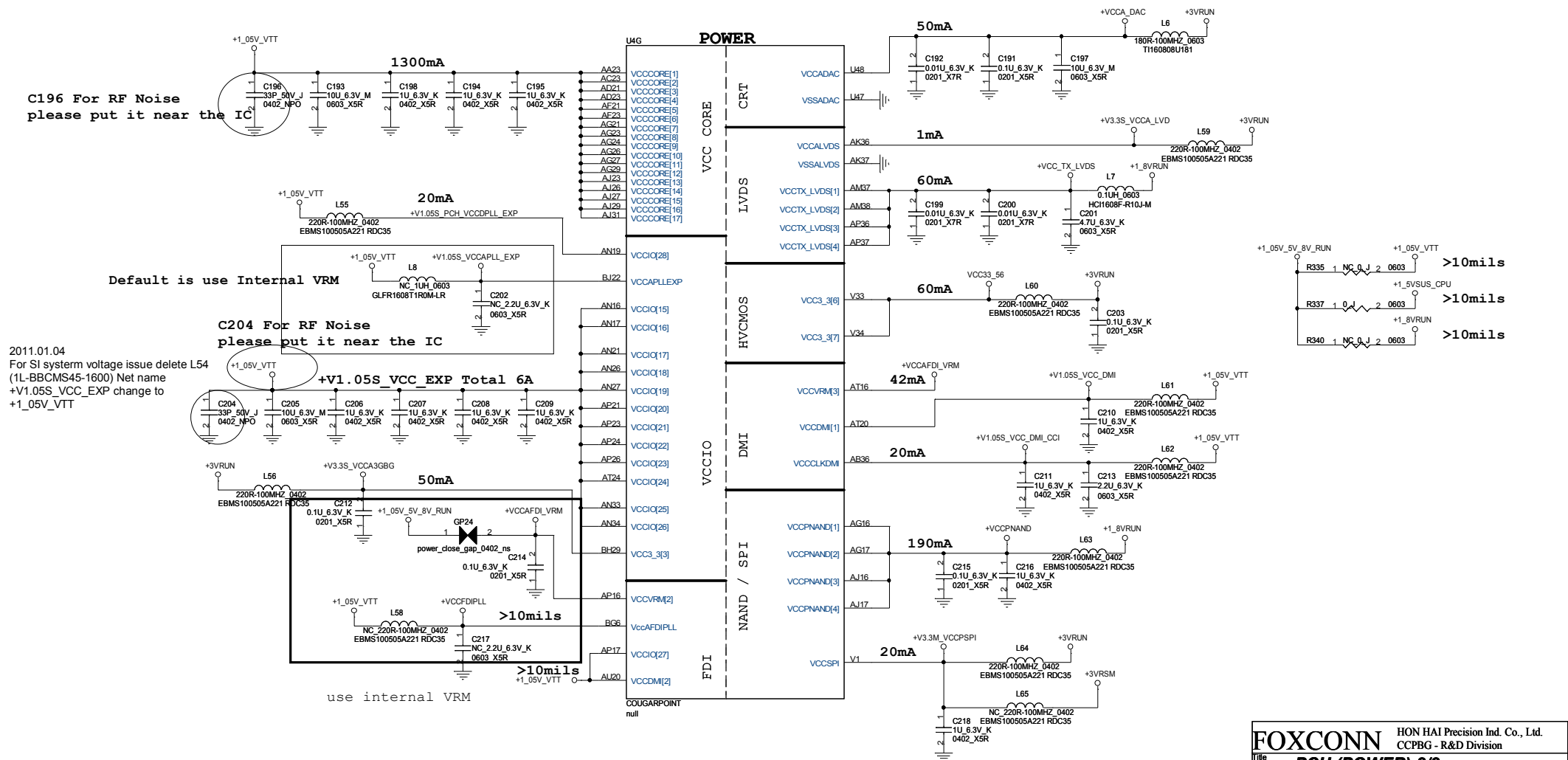
	3bit Value	SYSID2	SYSID1	SYSID0
EVT	110	H	H	L
Reserved	101	H	L	H
Reserved	100	H	L	L
Reserved	011	L	H	H
Reserved	010	L	H	L
Reserved	001	L	L	H
Reserved	000	L	L	L

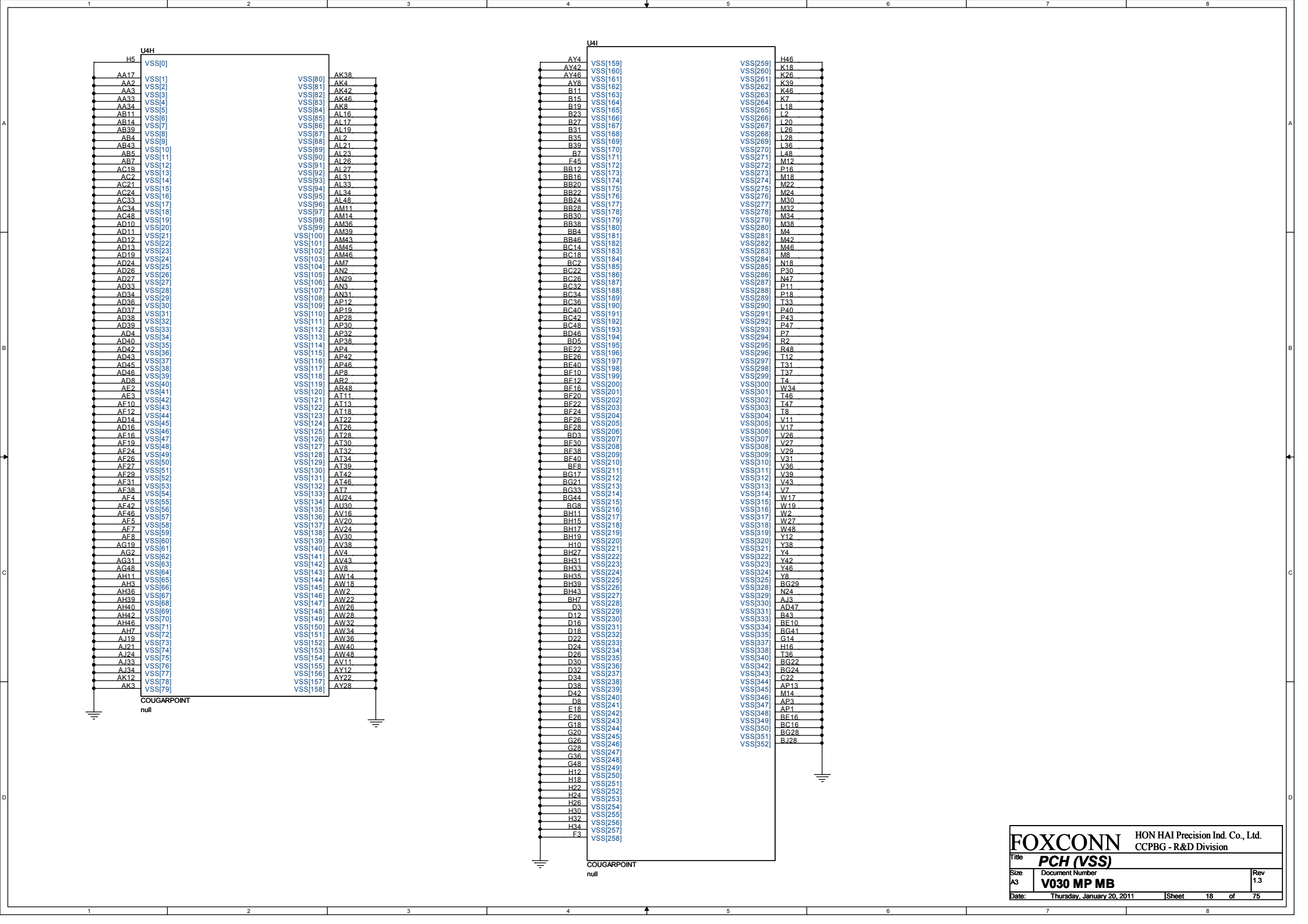


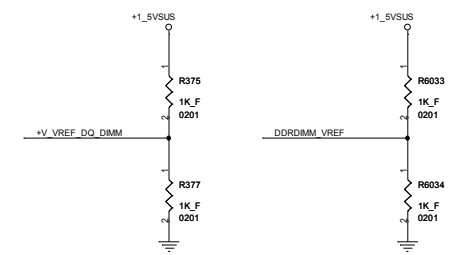
	4bit PRS	MEM PRS3	MEM PRS2	MEM PRS1	MEM PRS0
4GB (2Gb 16pcs)	0000	L	L	L	L
Reserved	0001	L	L	L	H
2GB (1Gb 16pcs)	0010	L	L	H	L
Reserved	0011	L	L	H	H
Reserved	0100	L	H	L	L
Reserved	0101	L	H	L	H
Reserved	0110	L	H	H	L
Reserved	0111	L	H	H	H



2010.1227
For quality issue 1C-33T0227-M102
forbit to use C148,C149 change to
1C-41T0227-M100







Place these Caps near So-DIMM0

+0.75V/RUN

C277
22P, 50V, J
0201_C0G

C278
1U, 6.3V, K
0402_XSR

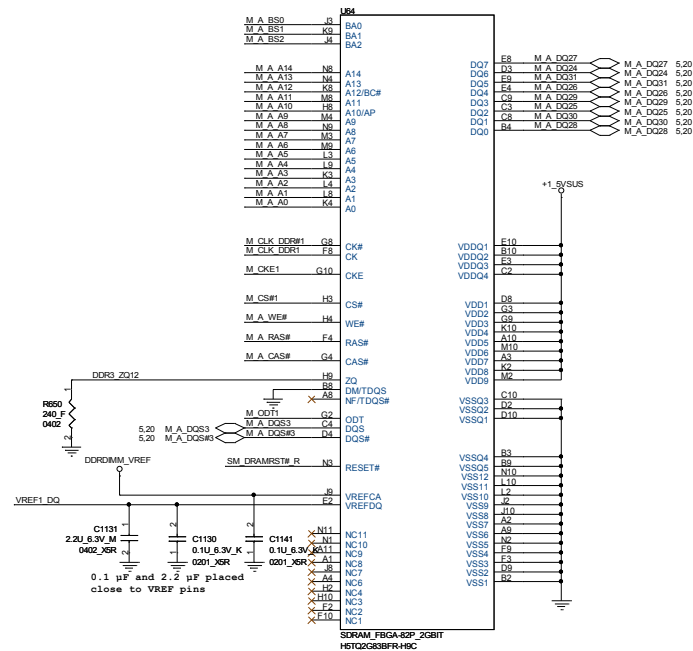
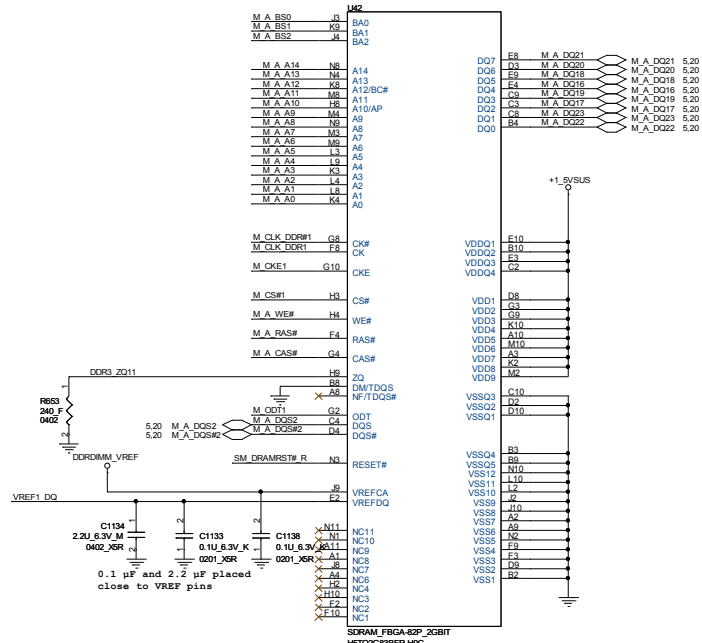
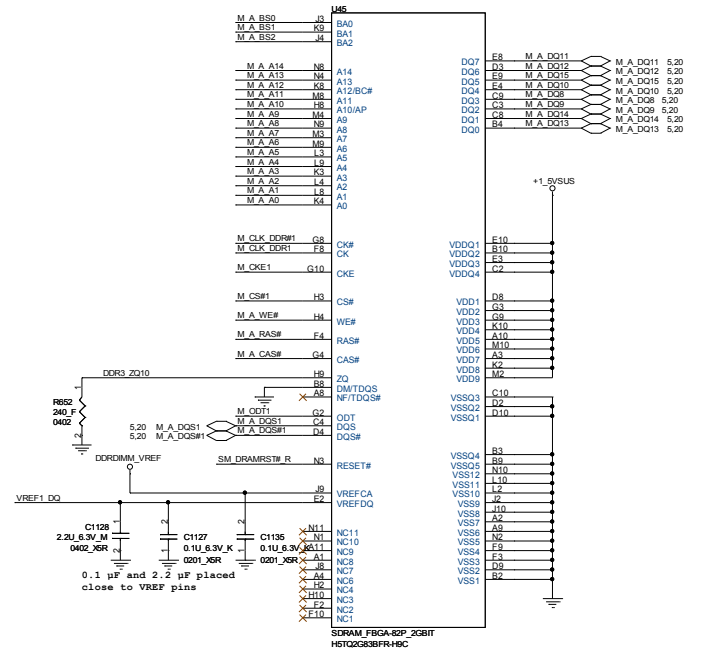
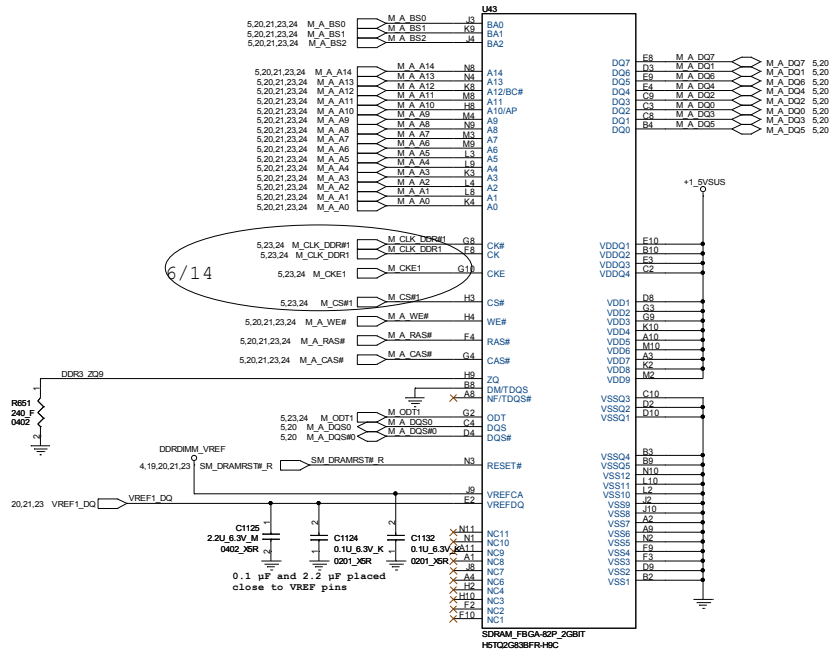
C279
1U, 6.3V, K
0402_XSR

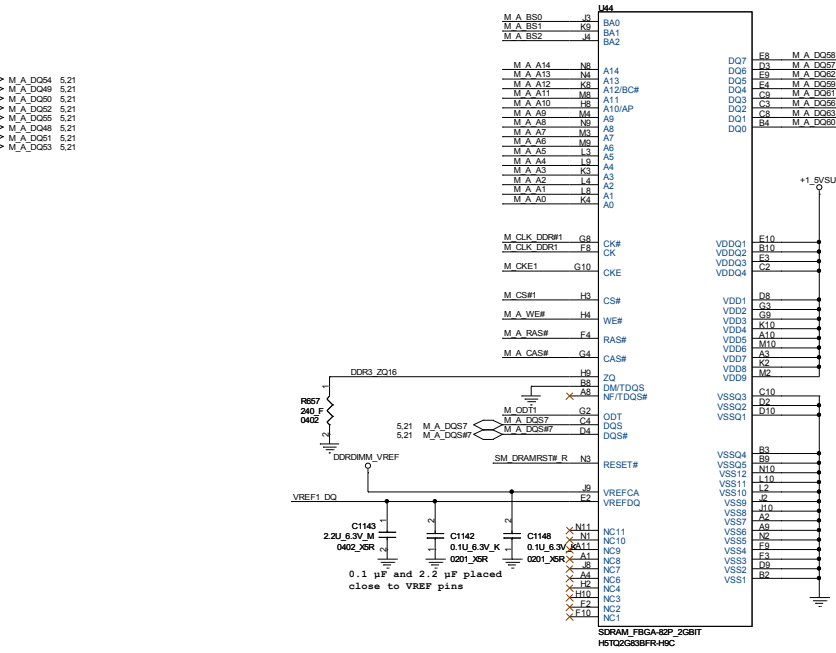
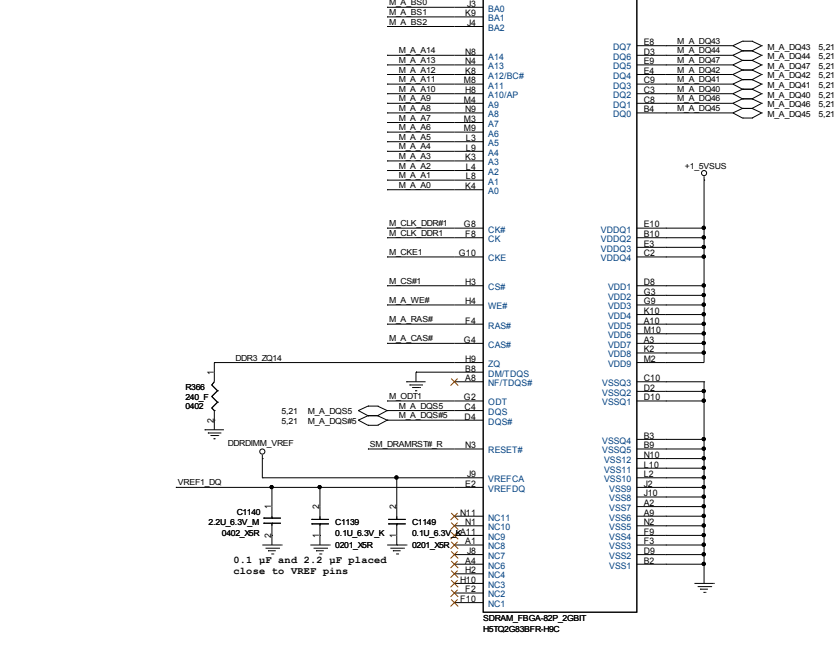
C280
1U, 6.3V, K
0402_XSR

C281
1U, 6.3V, K
0402_XSR

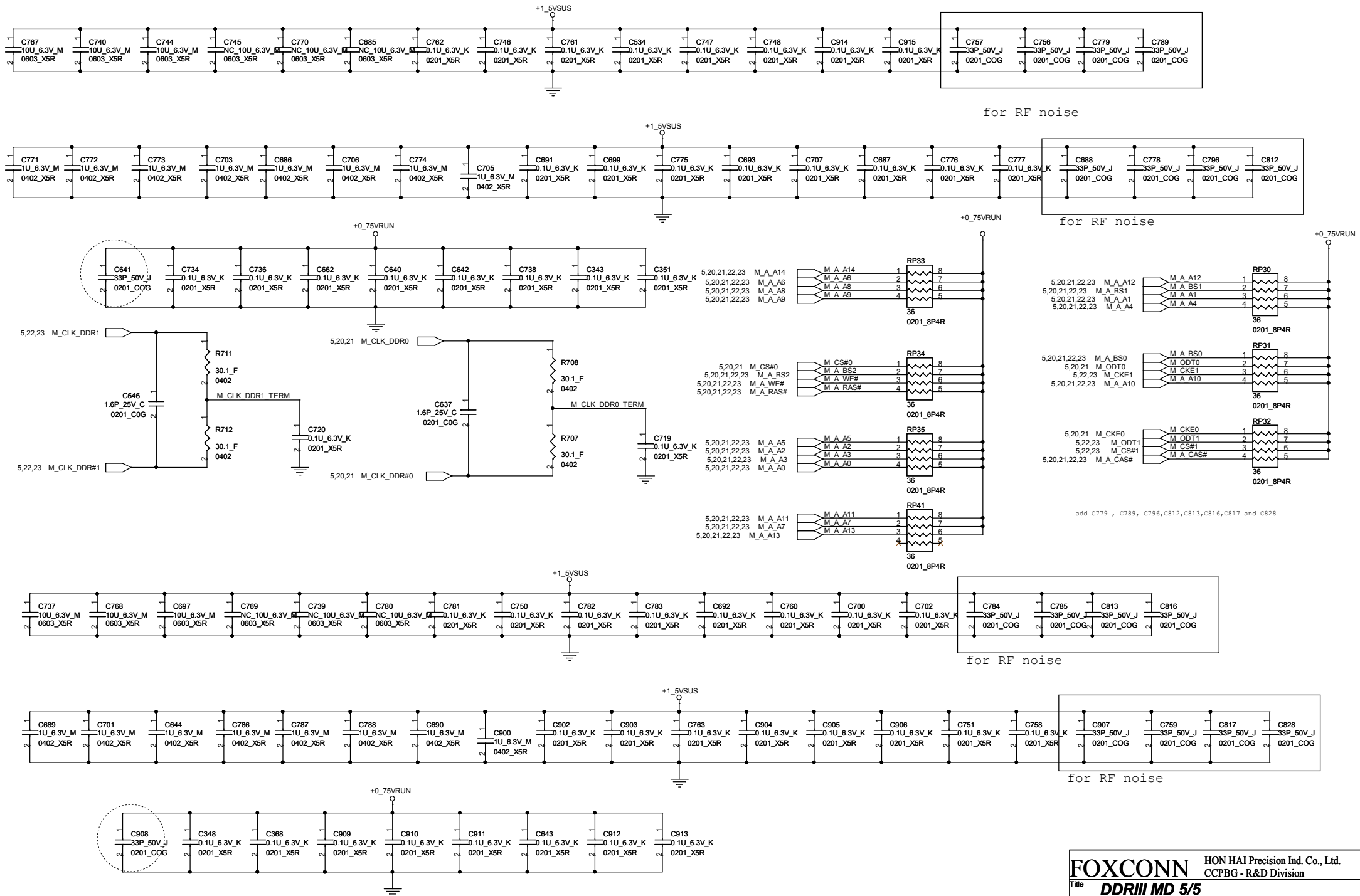
or RF Noise

For RF Noise



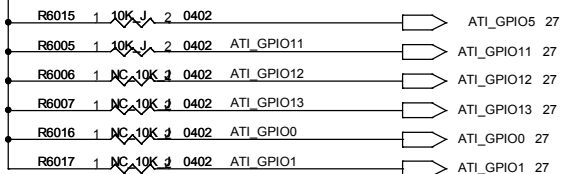


Place these caps close to MD



+3V3_DELAY

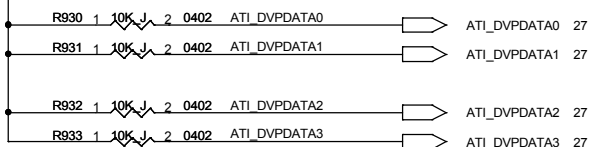
PIN STRAPS



If no ROM attached, GPIO[13:12:11]
CONFIG{2:0}
controls the memory aperture size.

64MB	010
128MB	000
256MB	001
512MB	not suport

+1_8VRUN_GPU



Strap for DDR3 VRAM
ATI_DVPDATA[3 : 0]

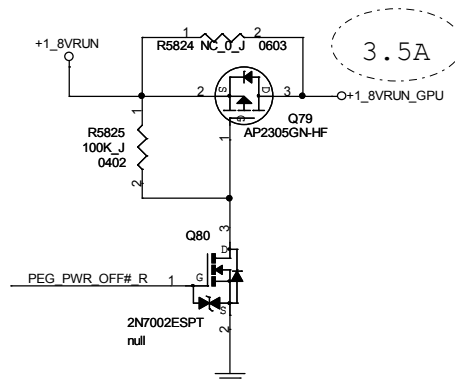
For Seymour XT / Robson XT

0001	64Mx16	Hynix	: H5TQ1G63BFR-12C (Orion-die)	x4pcs
0010	64Mx16	Samsung	: K4W1G1646E-HC12 (E-die)	x4pcs
0011	64Mx16	Reserve	for Nanya	x4pcs
0100	128Mx16	Hynix	: H5TQ2G63BFR-12C (Vega-die)	x4cps
0101	128Mx16	Samsung	: K4W2G1646B-HC12 (B-die)	x4pcs
0110	128Mx16	Reserve	for Nanya	x4pcs
0111	128Mx16	Micron	: MT41J128M16HA-12 (Rev D)	x4pcs

For Whistler LP

0001	64Mx16	Hynix	: H5TQ1G63BFR-12C (Orion-die)	x8pcs
0010	64Mx16	Samsung	: K4W1G1646E-HC12 (E-die)	x8pcs
0011	64Mx16	Reserve	for Nanya	x8pcs
0100	128Mx16	Hynix	: H5TQ2G63BFR-12C (Vega-die)	x8pcs
0101	128Mx16	Samsung	: K4W2G1646B-HC12 (B-die)	x8pcs
0110	128Mx16	Reserve	for Nanya	x8pcs
0111	128Mx16	Micron	: MT41J128M16HA-12 (Rev D)	x8pcs

P.S. * means Hynix H5TQ1G63BFR-12C, 800MHZ
**means Samsung K4W1G1646E-HC12T00, 800MHZ
***means Elpida EDJ1116DBSE-DJ-F, 1333MHz
****means AMD 23EY2387MA-12, 800MHZ



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET

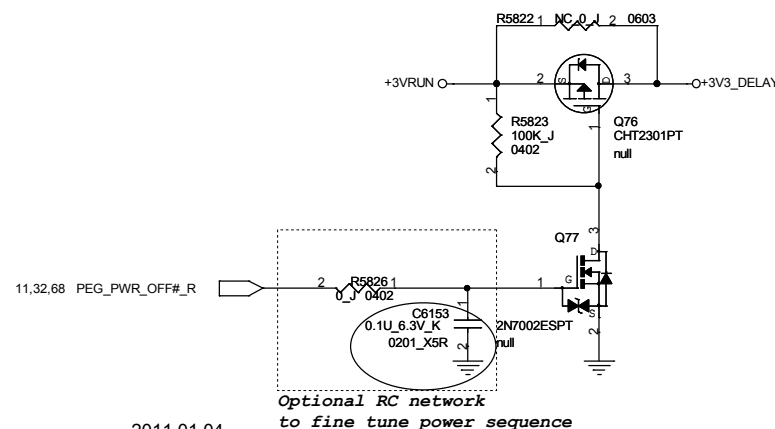
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN name	DESCRIPTION OF DEFAULT SETTINGS
TX_PWRS_ENB	GPIO_0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing
AC_BATT	GPIO_5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V
PWRCNTL_0 PWRCNTL_1	GPIO_15 GPIO_20	At Reset, these signals will be inputs with weak internal pull-down resistors. VBIOS can define these signals to be either 3.3-V outputs or open drain outputs. The output state (high/low) of these signals is programmable for each PowerPlay state.
SSIN	GPIO_16	Spread Spectrum clock input for memory clock and/or engine clock (maximum down spread of -2.5%). Requires a spread version of 27 MHz(The modulation rate is 30-50 KHz.)
THERMAL_INT	GPIO_17	Thermal monitor interrupt Can be set as either: 1) An input from an external temperature sensor (ALERTb) , or 2) An output signaling that the ASIC temp (measured by the internal sensor) is above the high threshold or below the low threshold.Output can be open drain or 3.3-V output.(active low by default)

GPIO_0: Tx output swing half / full

GPIO_1: Tx deemphasis disable / enable

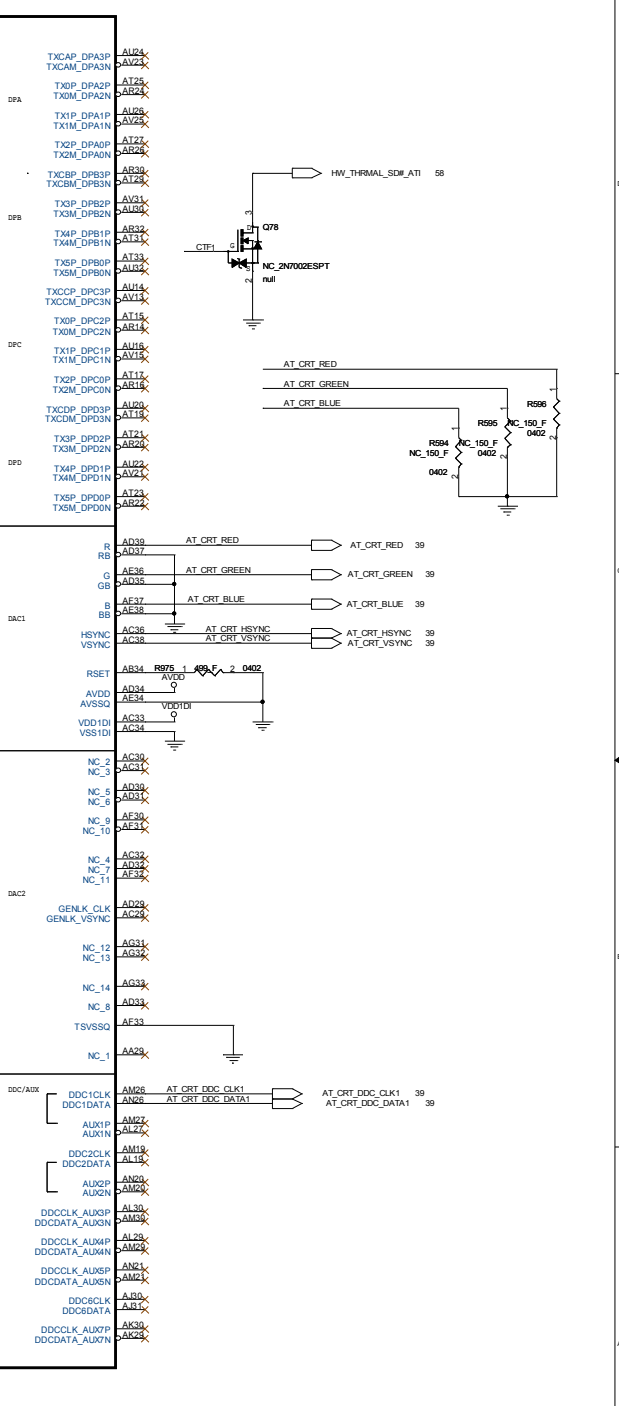
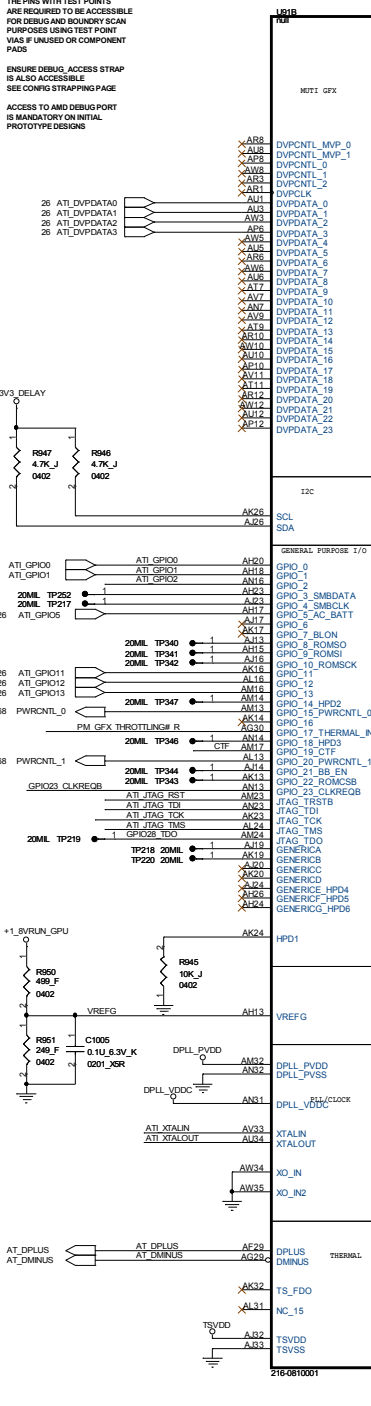
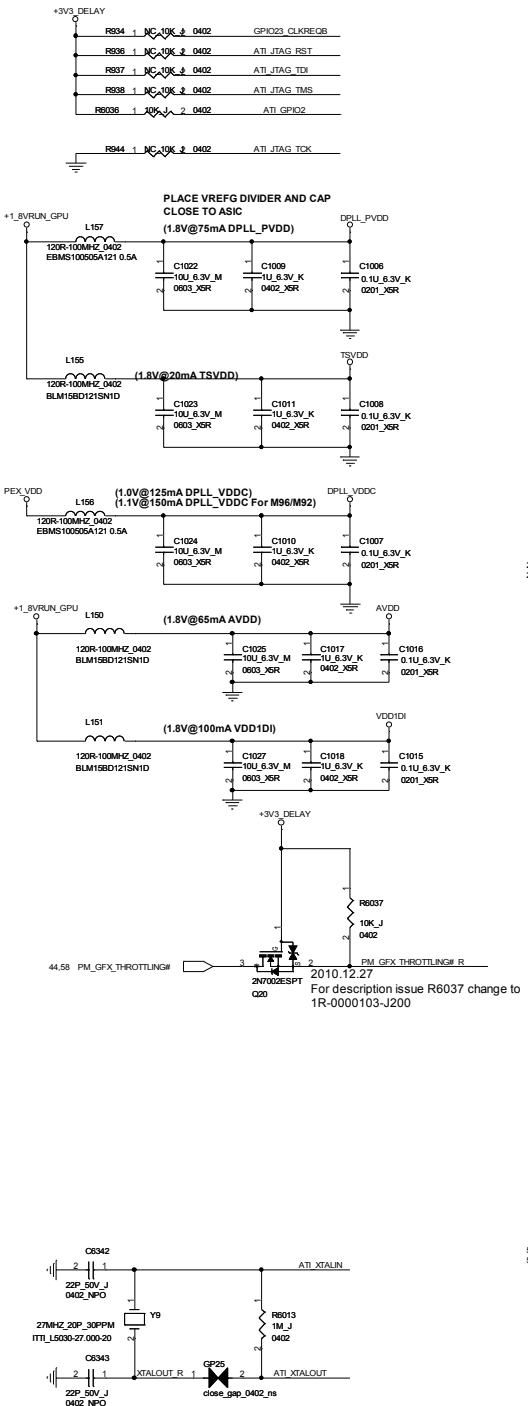
Co-layer for R5822 and Q76 pin2,3



2011.01.04

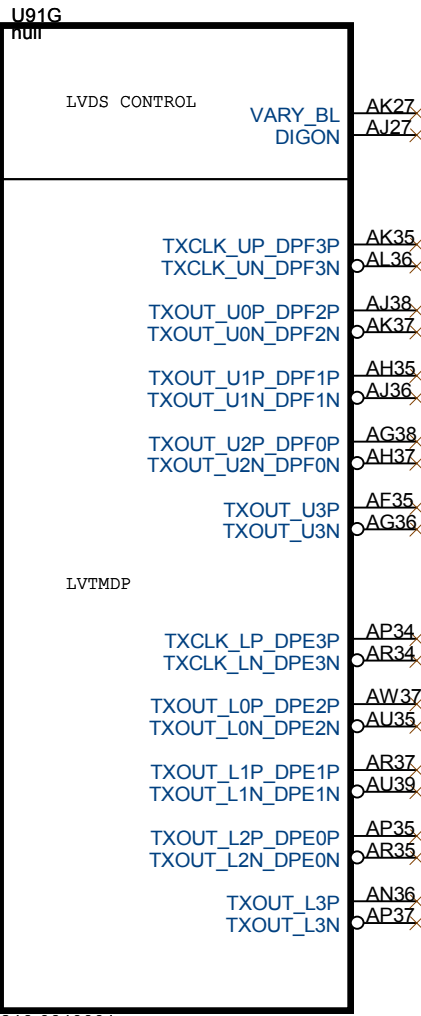
For +3VRUN voltage drop issue NPIT suggest C6153
change to mount

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
VGA (Straps) 2/8			
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B	V030 MP MB		1.3
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5.3.1 Switchable Graphics - 27-MHz Clock for DGPU
DGPU's requiring a 27MHz clock in a Switchable Graphics configuration shall have to use a discrete crystal and should not source this clock from the PCH. This restriction does not apply to Discrete-graphics only systems. Refer to the WW10 Huron River Platform Message of the week for more details.

LVDS Interface



AK27
AJ27

AK35
AL36

AJ38
AK37

AH35
AJ36

AG38
AH37

AF35
AG36

AP34
AR34

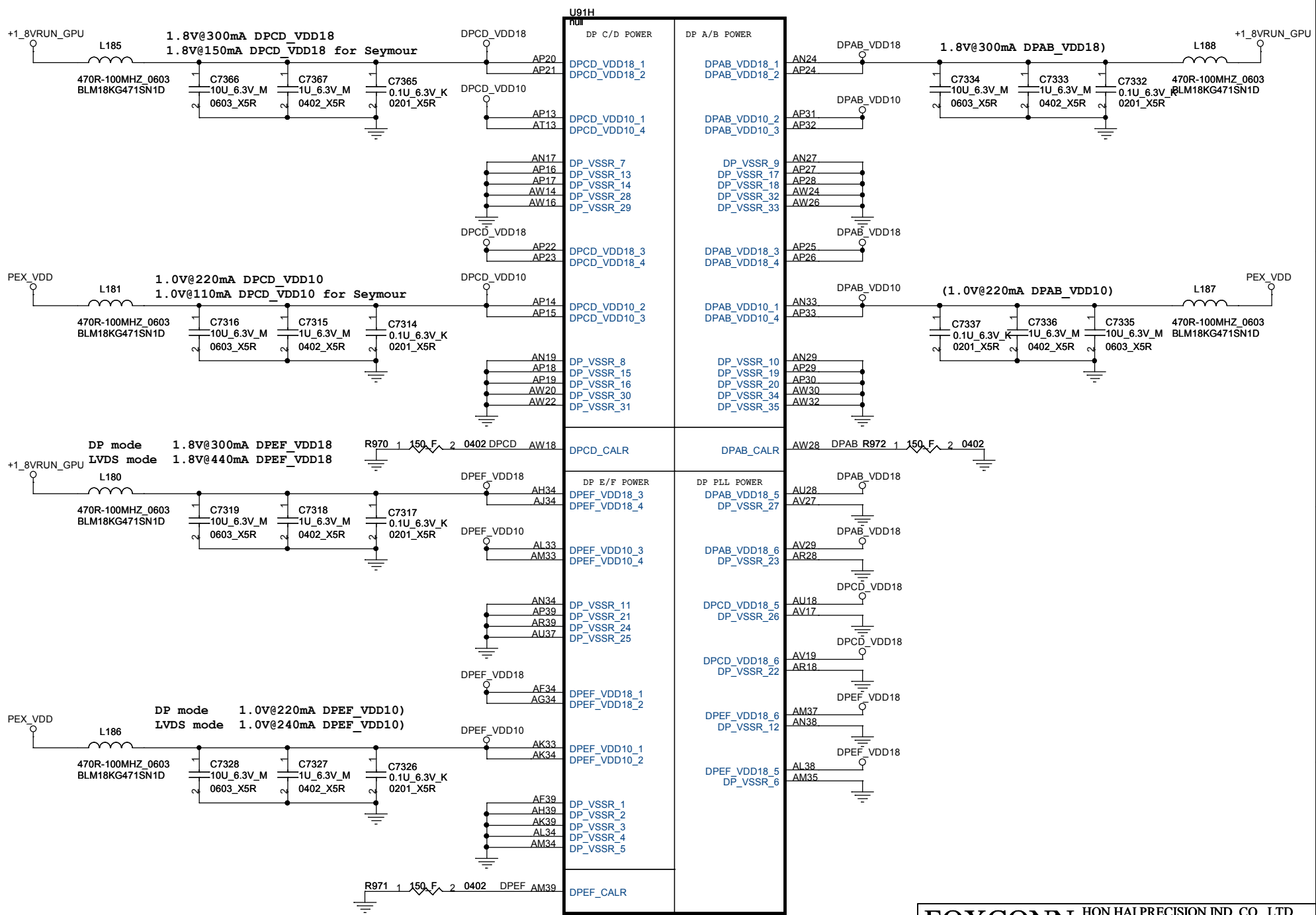
AW37
AU35

AR37
AU39

AP35
AR35

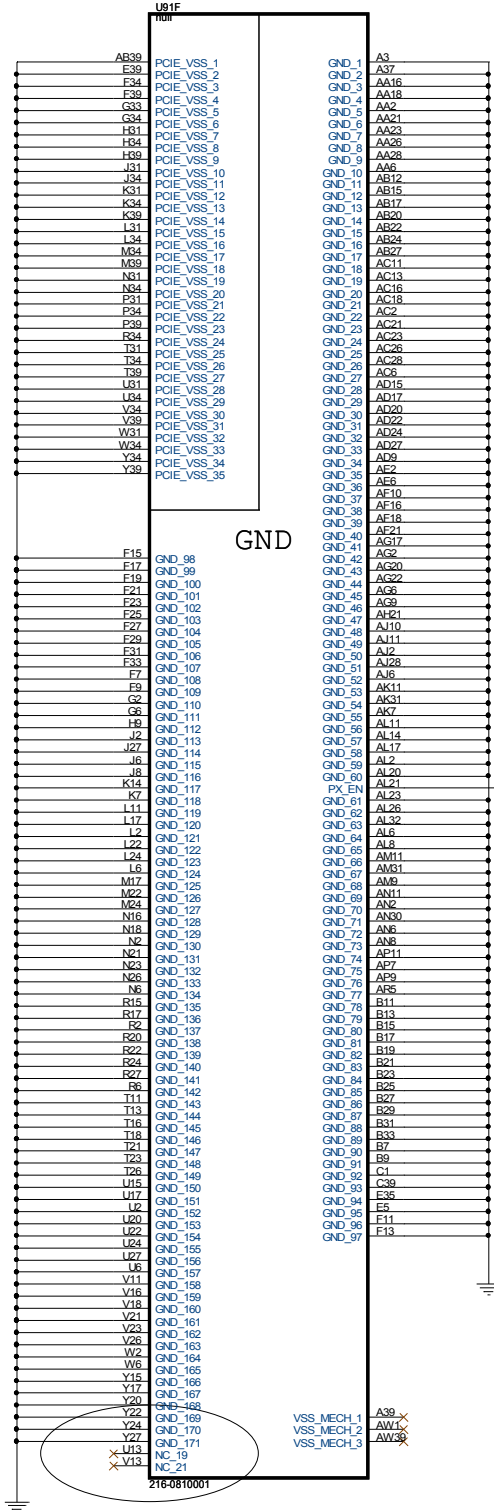
AN36
AP37

FOXCONN		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title VGA (LVDS) 5/8			
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R970/R971/R972 close to U91
change R970/R971/R972 precision from 5% to 1%
for follow check list 2010/06/04

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
VGA (power2) 7/8			
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PX_MODE =1, for Normal Operation
PX_MODE =0, for BACO MODE

PX_EN =0, for Normal Operation
PX_EN =1, for BACO MODE

For PX_EN, refer to the BACO reference schematics for detail

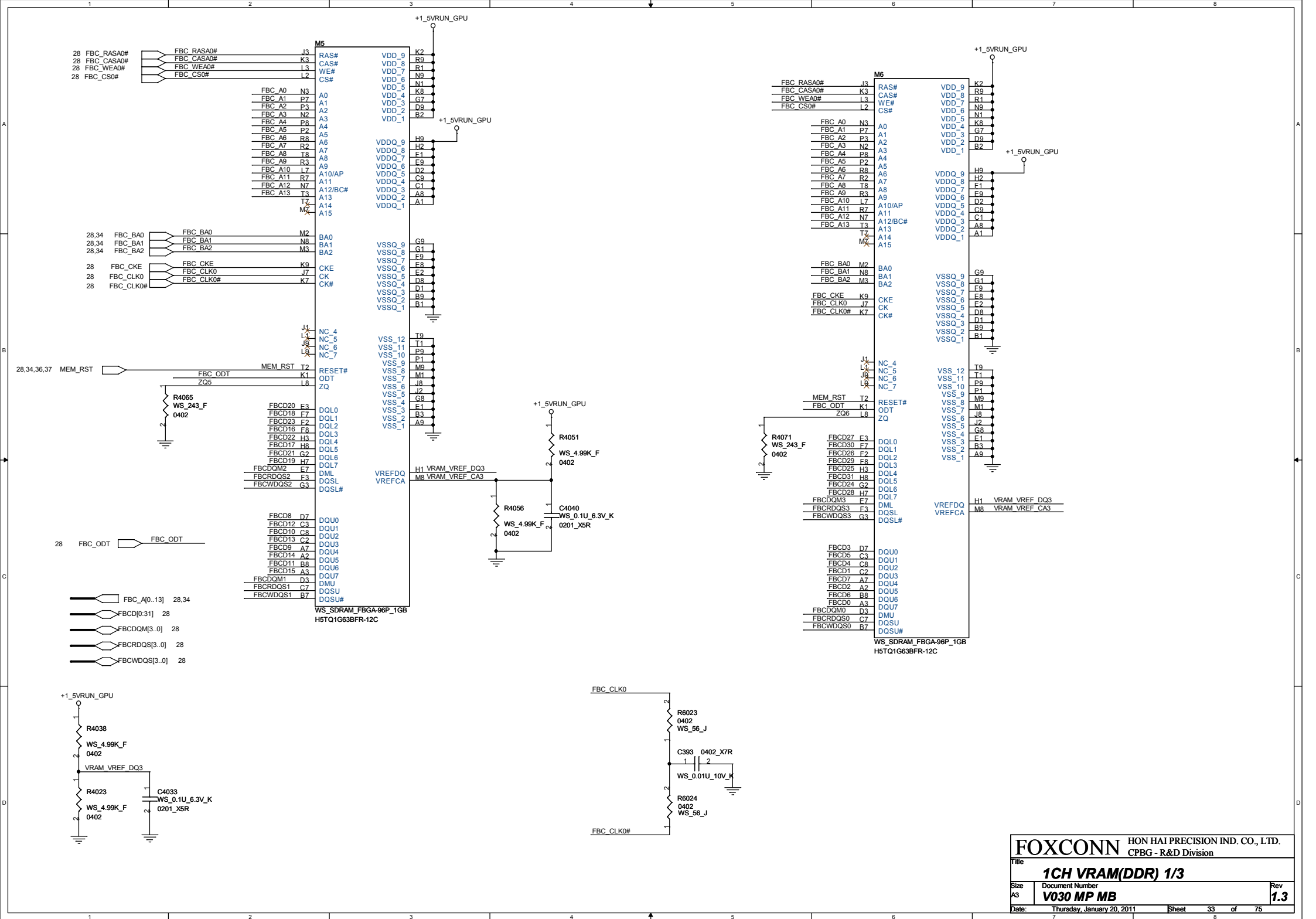
add R935 for follow check list 2010/06/04
Dummy R935 for follow NDA_1.02 201011/25

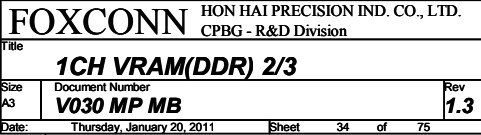
For PX3 mode, install R941
and remove Q190, Q191, Q192, Q193, Q194, Q496, U19, C246, R926, R927 and R929.
2010/11/22

In preparation for the case of
do not support the BACO option,
please connect the BIF_VDDC
to AT_VDD with 0ohm resistor.
0 ohm resistor is NC. 6/17

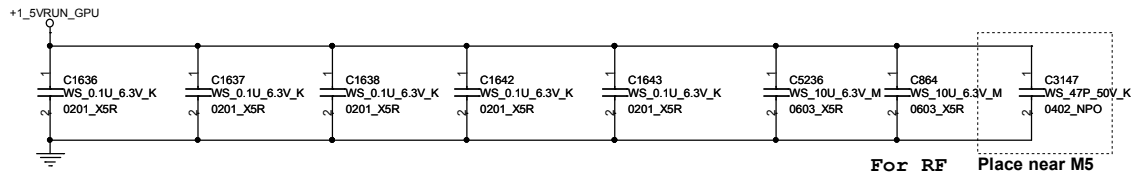
BIF_VDDC: current consumption = 55mA@1.0V,
in BACO mode

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
VGA (GND) 8/8			
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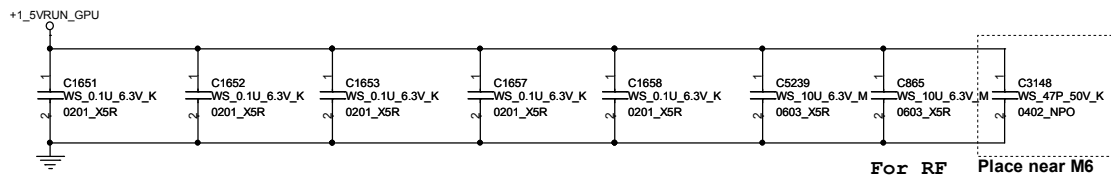




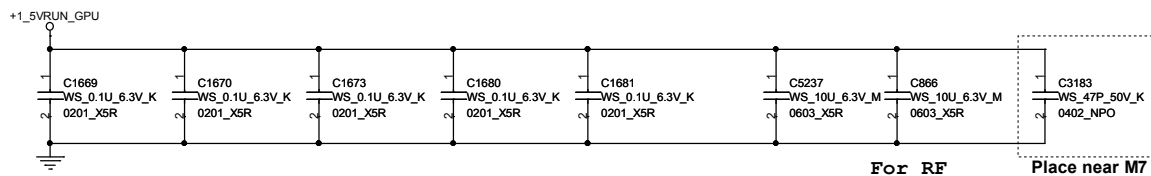
Place around the VRAM M5



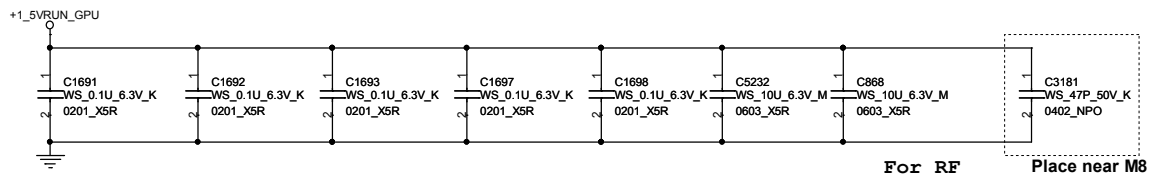
Place around the VRAM M6



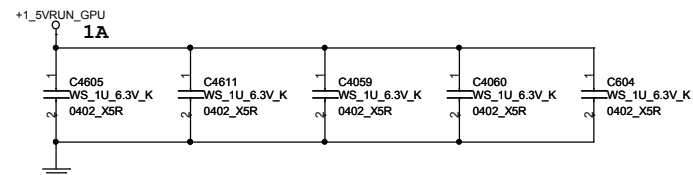
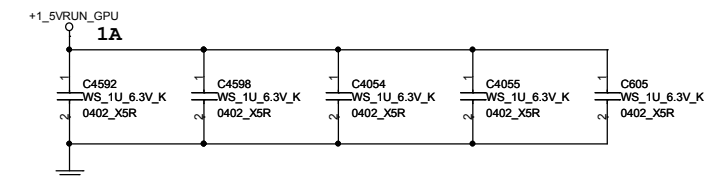
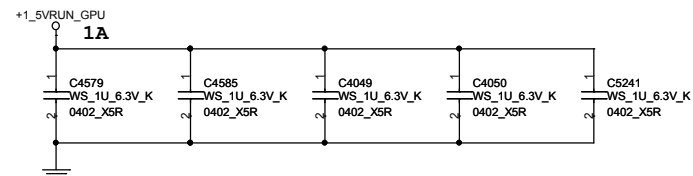
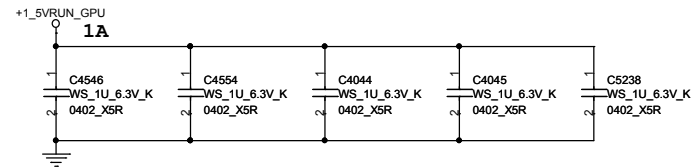
Place around the VRAM M7



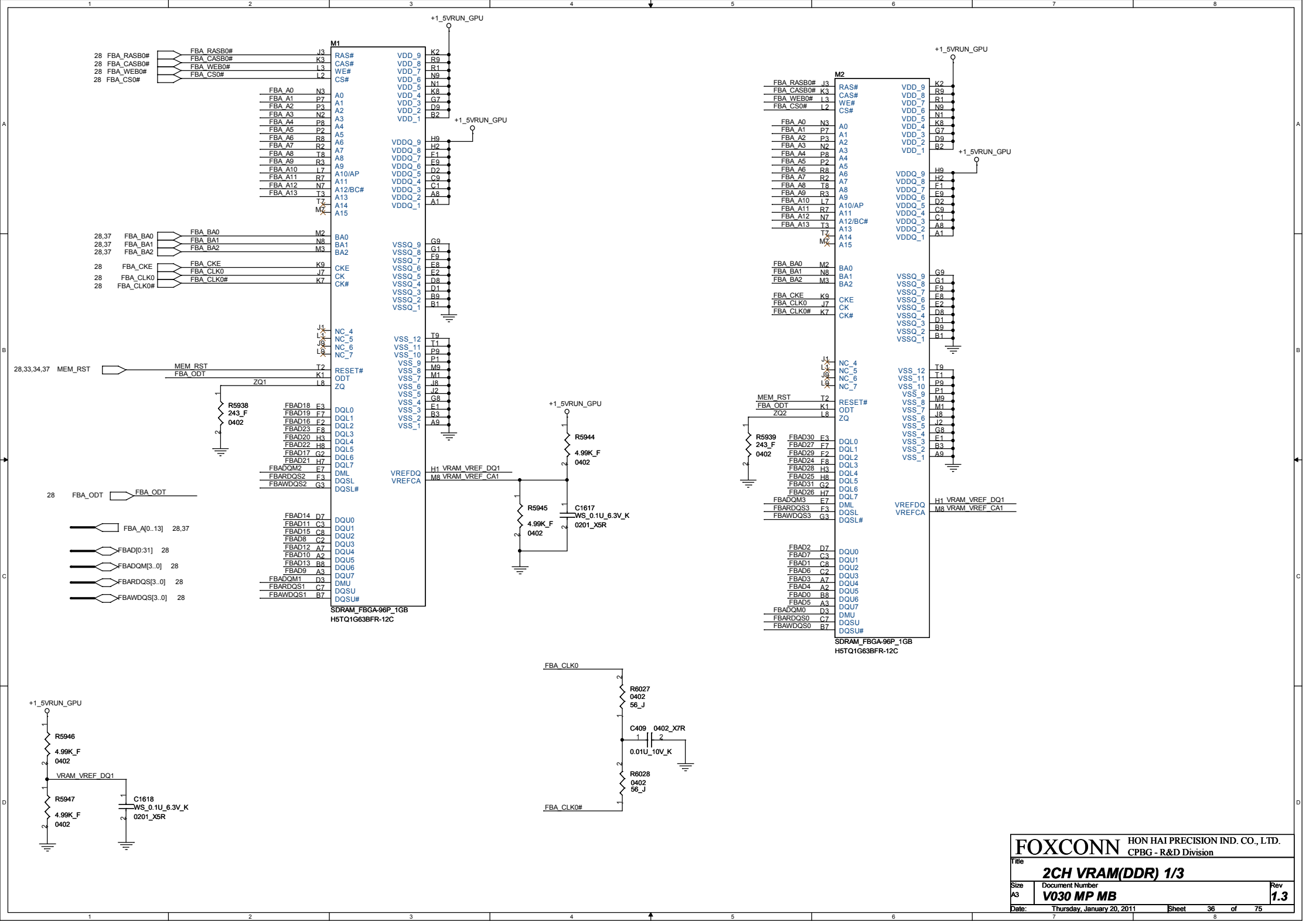
Place around the VRAM M8

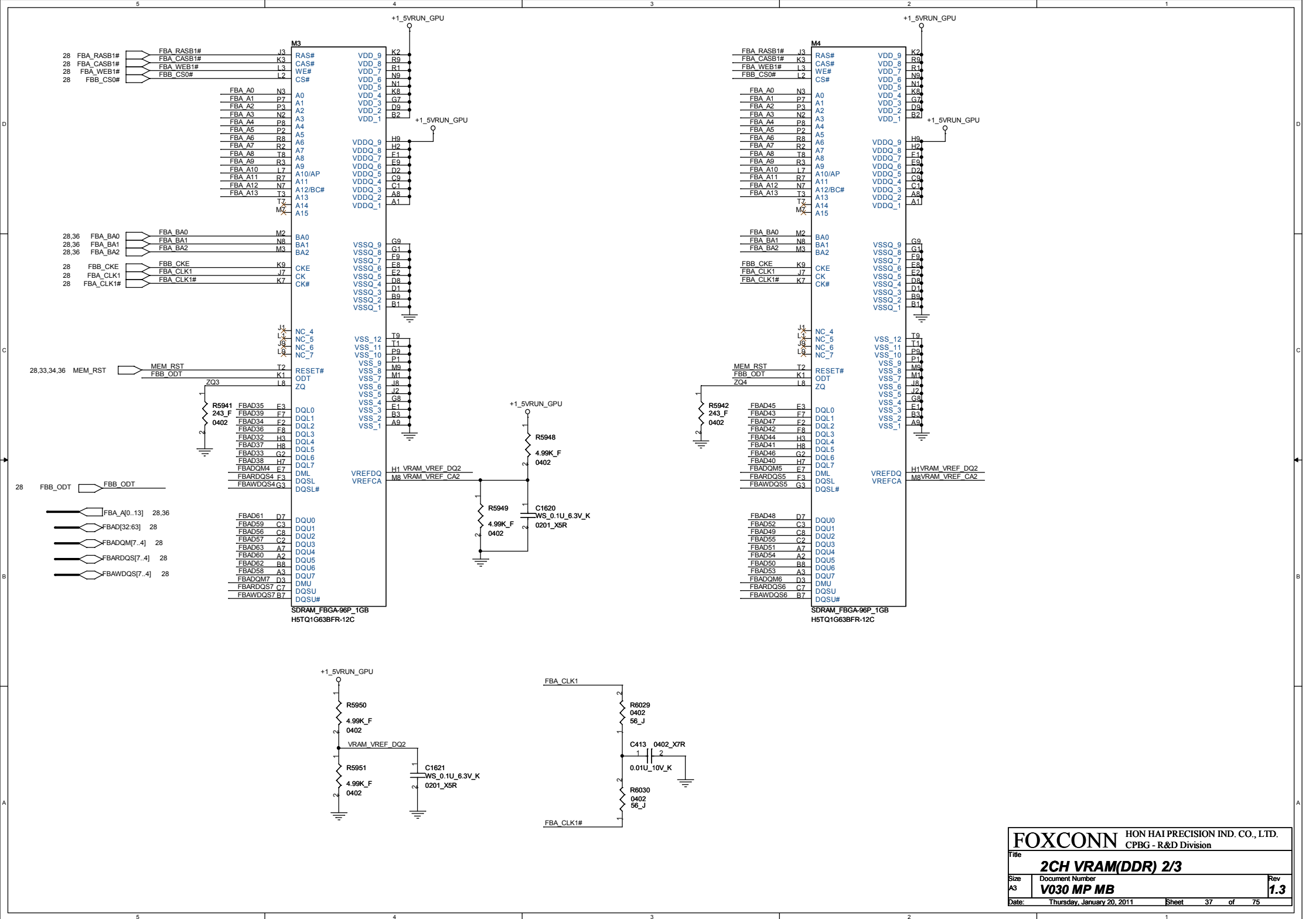


PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

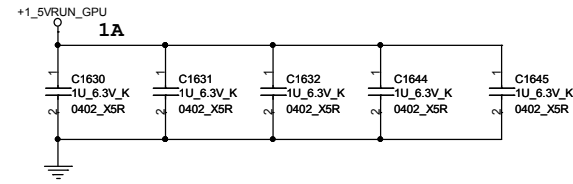
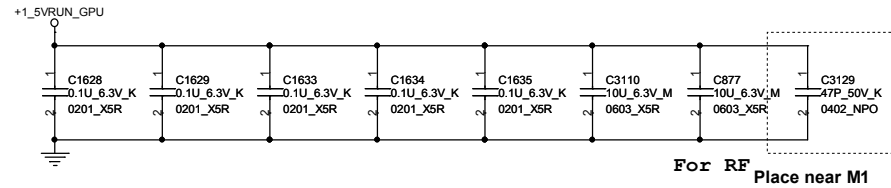


PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

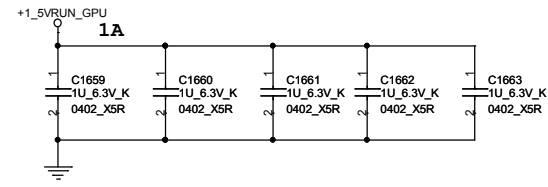
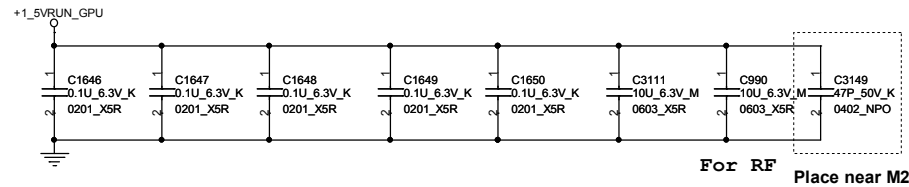




Place around the VRAM M1

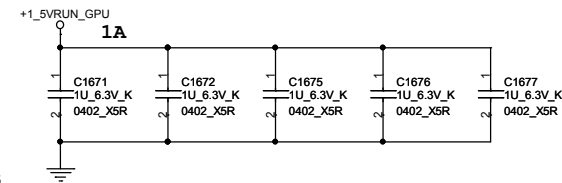
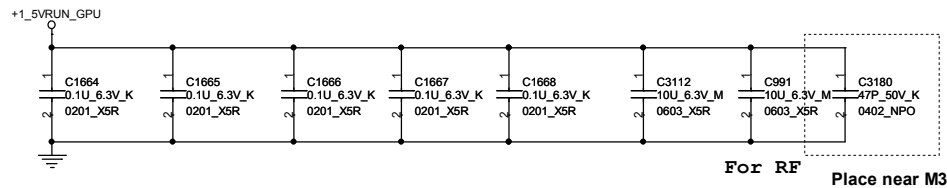


Place around the VRAM M2

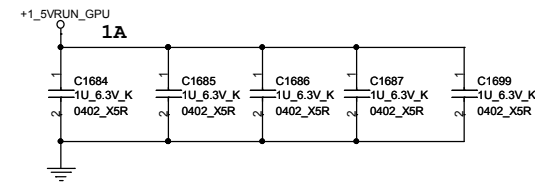
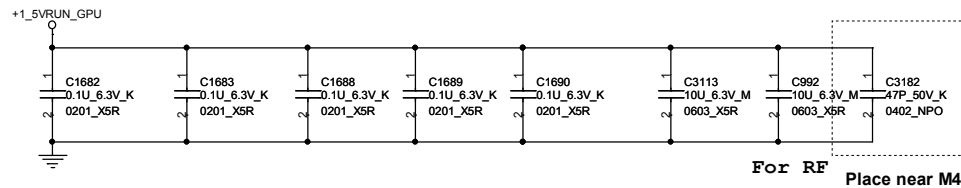


change C3110,C3111,C3112,C3113,C877,C990,C991 and C992 to 10u 0702

Place around the VRAM M3

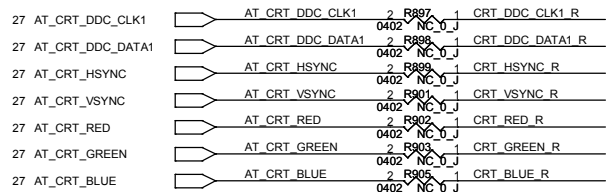
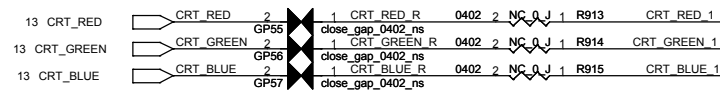
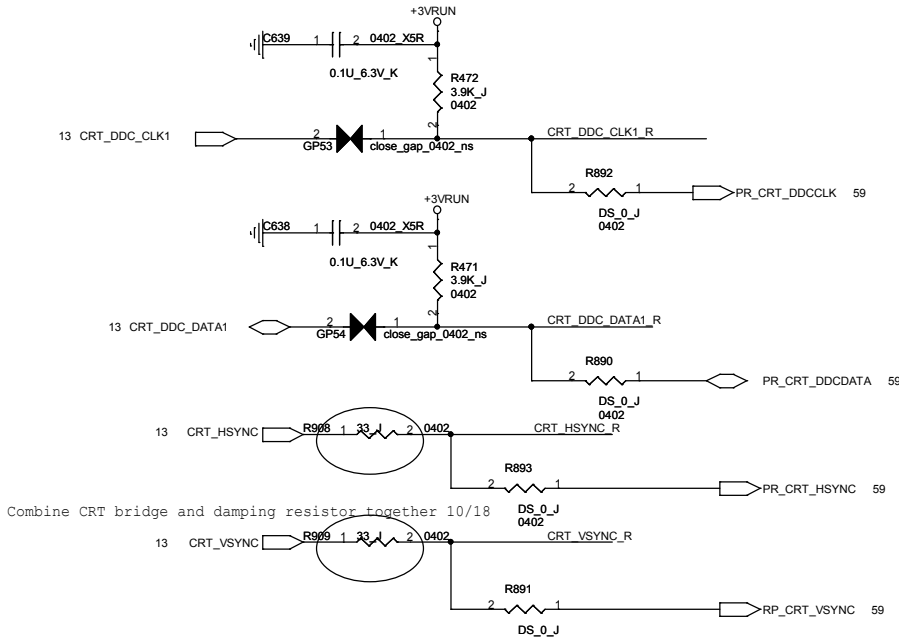


Place around the VRAM M4



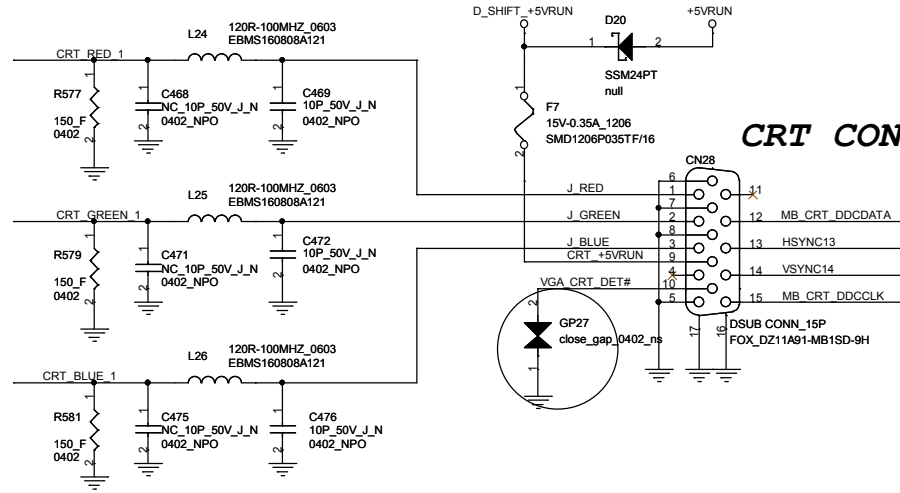
PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

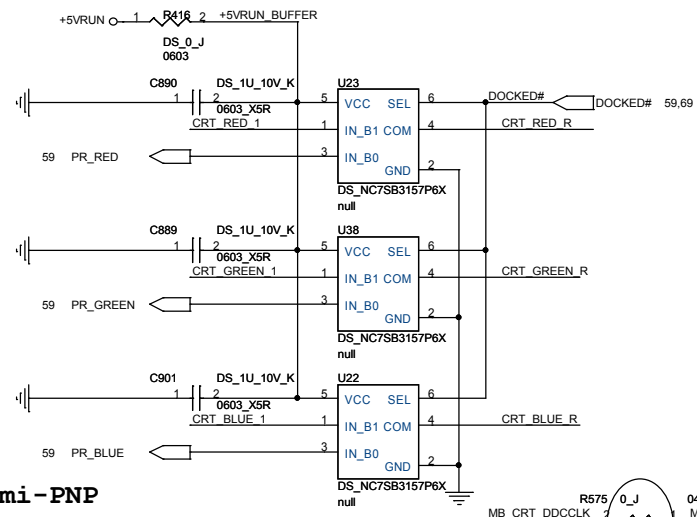
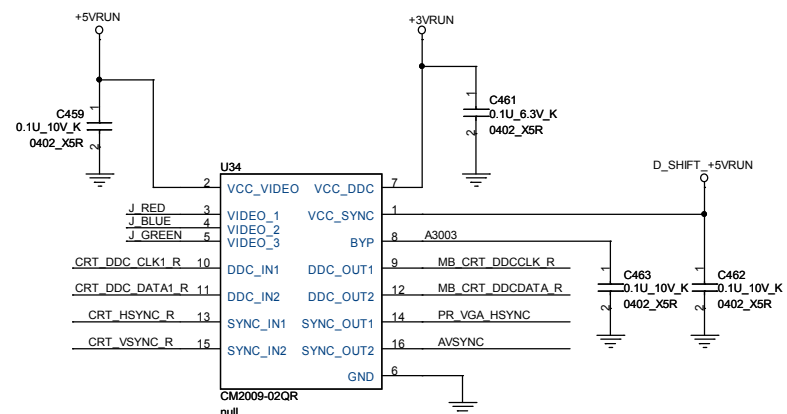


ND_ means no DOCKing and
DS_ means has docking

For WIN 7, delete Semi-PNP

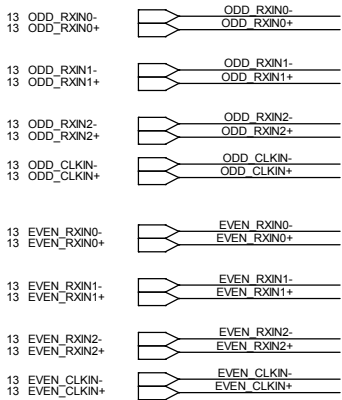


CRT CONNECTOR

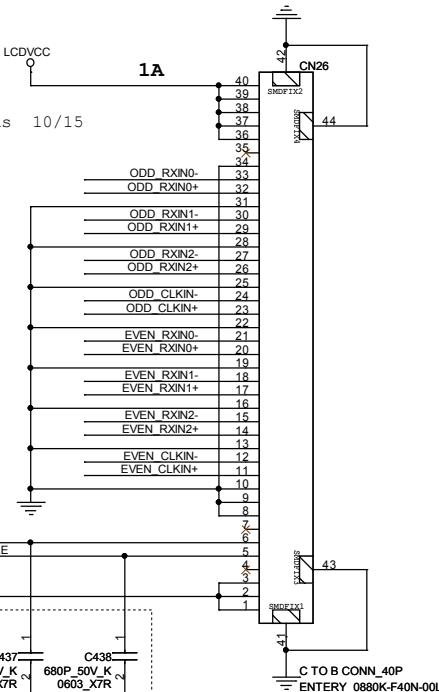


For EMI

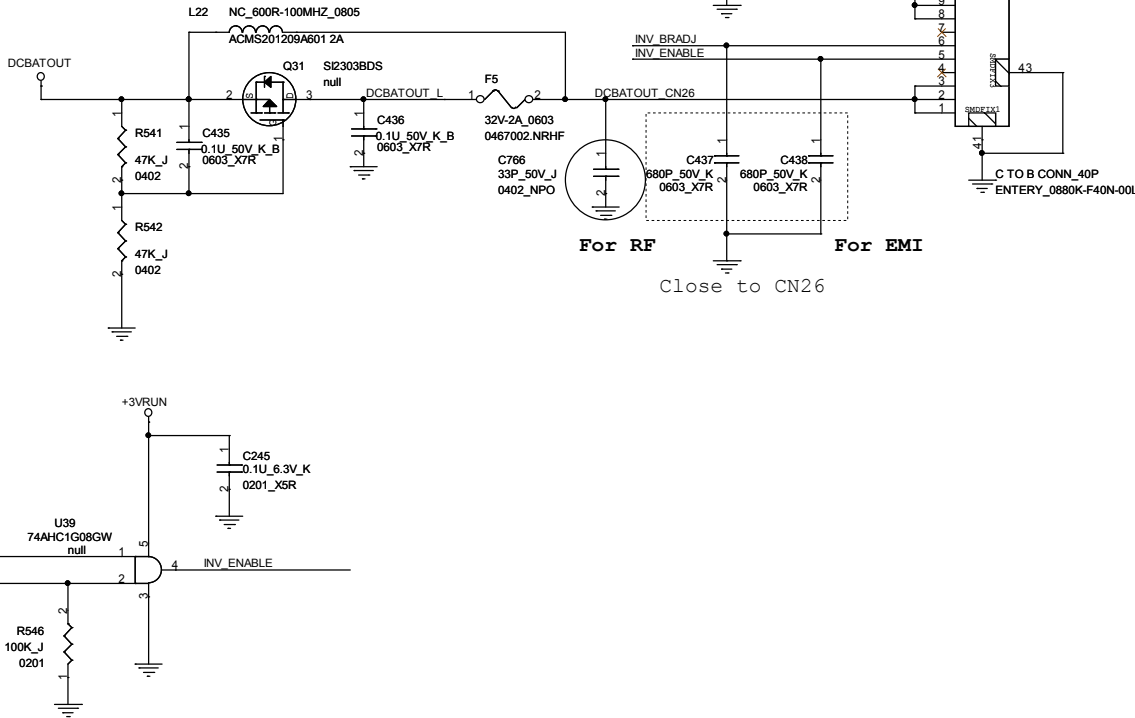
LVDS CONNECTOR



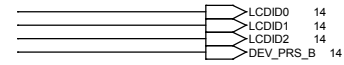
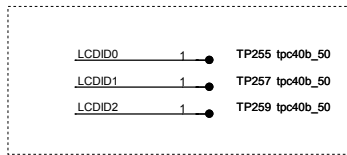
MOR request change to 1A, and need add power pins 10/15



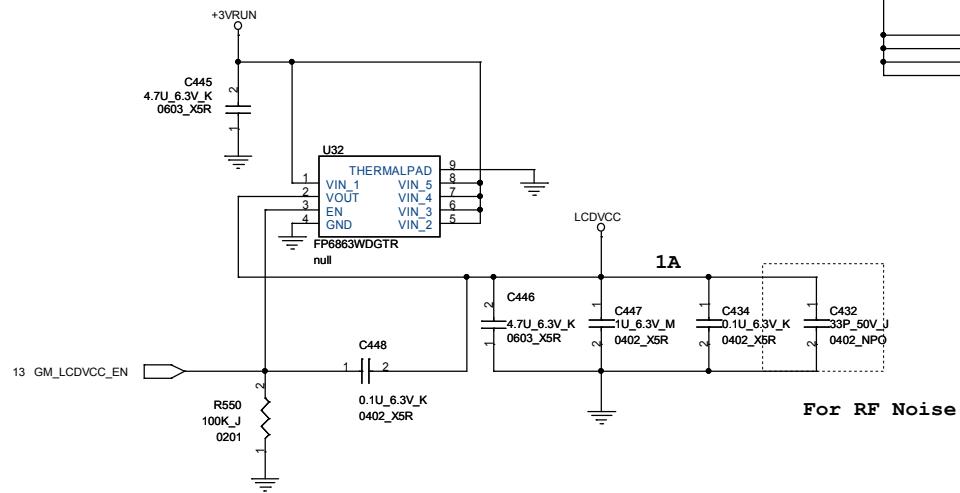
For rush current issue



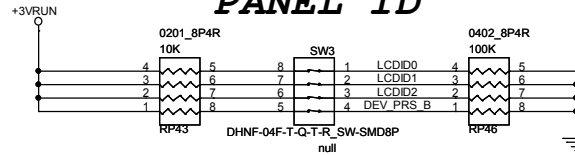
Bot-Side



LCDVCC Power



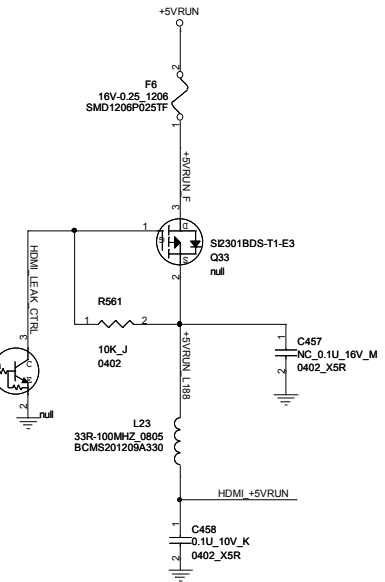
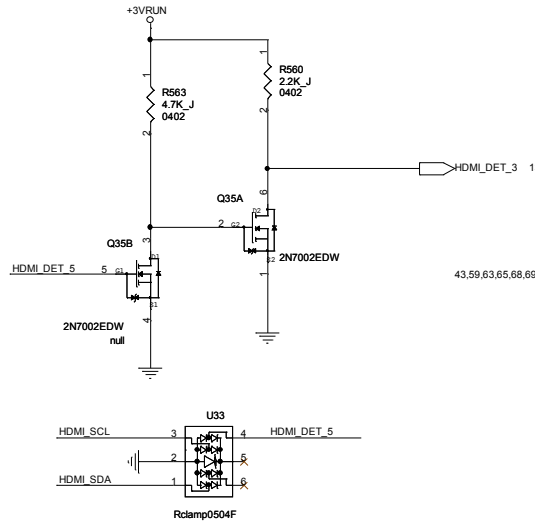
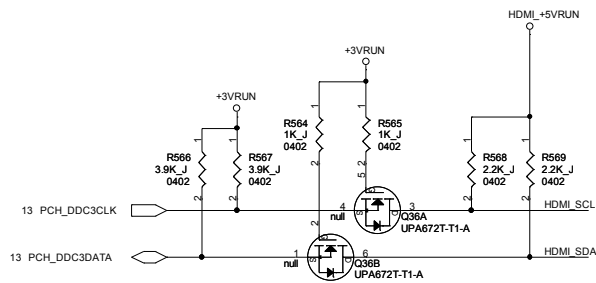
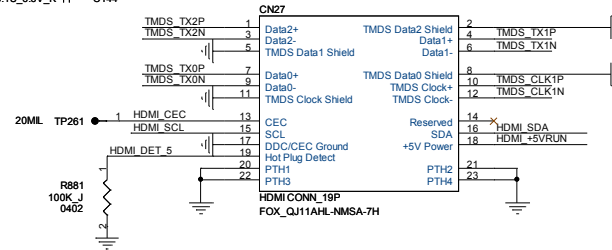
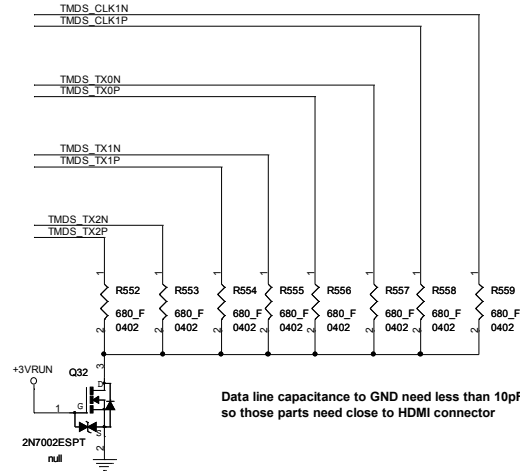
PANEL ID

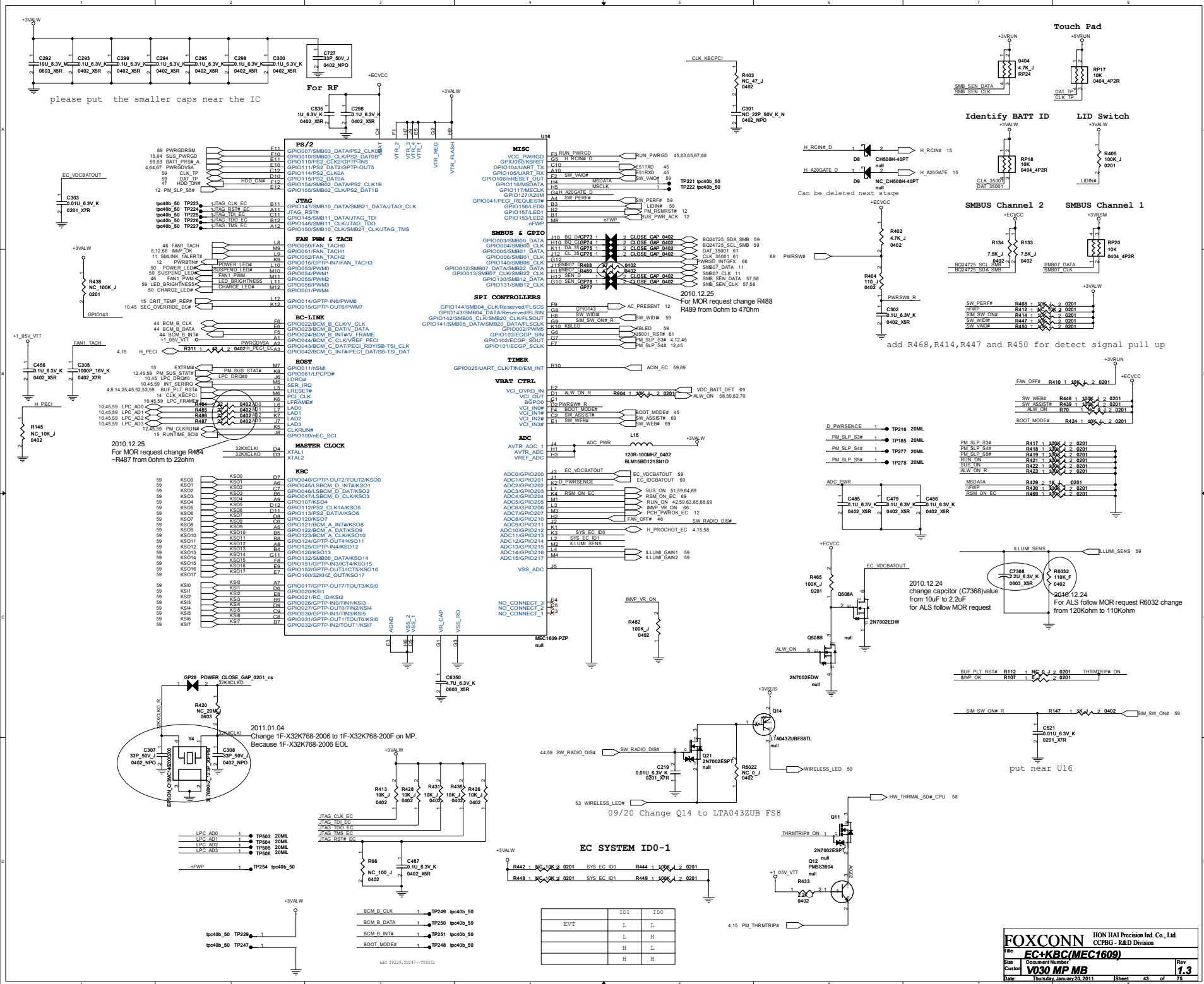


SW1 (Panel ID)	LCDID2	LCDID1	LCDID0
CRT (No LCD)	0	0	0
CMI 1366x768	0	0	1
AUO 1366x768	0	1	0
CPT 1366x768	0	1	1
CPT 1600x900	1	0	0
RESERVED	1	0	1
RESERVED	1	1	0
RESERVED	1	1	1

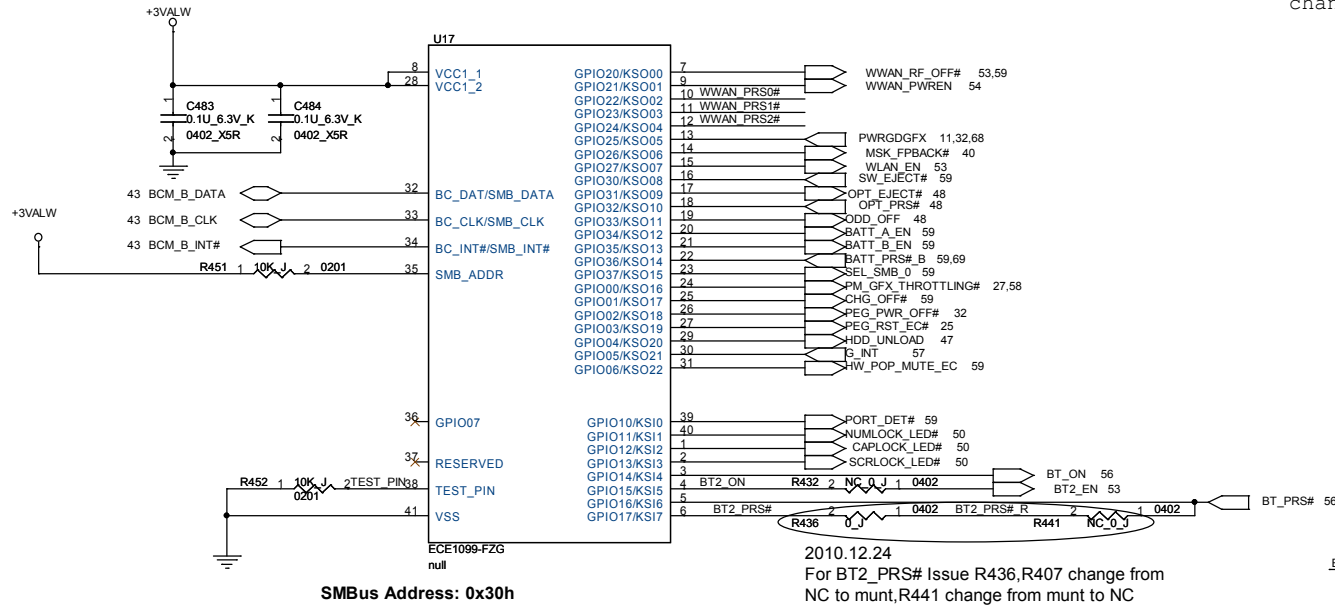
ON:1 , OFF:0

13	TMDS_DATA0#_C	TMDS_DATA0#_C	0201_X5R	0.1U_6.3V_K	2	1	TMDS_TX0N
13	TMDS_DATA0_C	TMDS_DATA0#_C	0201_X5R	0.1U_6.3V_K	2	1	TMDS_TX0P
13	TMDS_DATA1#_C	TMDS_DATA1#_C	0201_X5R	0.1U_6.3V_K	2	1	TMDS_TX1N
13	TMDS_DATA1_C	TMDS_DATA1#_C	0201_X5R	0.1U_6.3V_K	2	1	TMDS_TX1P
13	TMDS_DATA2#_C	TMDS_DATA2#_C	0201_X5R	0.1U_6.3V_K	2	1	TMDS_TX2N
13	TMDS_DATA2_C	TMDS_DATA2#_C	0201_X5R	0.1U_6.3V_K	2	1	TMDS_TX2P
13	TMDS_CLK#_C	TMDS_CLK#_C	0201_X5R	0.1U_6.3V_K	2	1	TMDS_CLK1N
13	TMDS_CLK_C	TMDS_CLK#_C	0201_X5R	0.1U_6.3V_K	2	1	TMDS_CLK1P





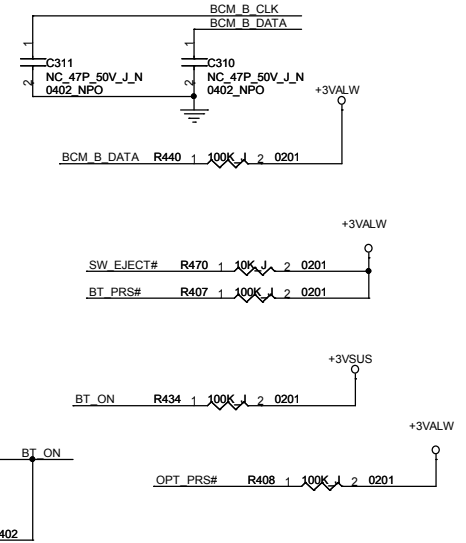
add C483 and C484 following vendor's suggestion.6/29



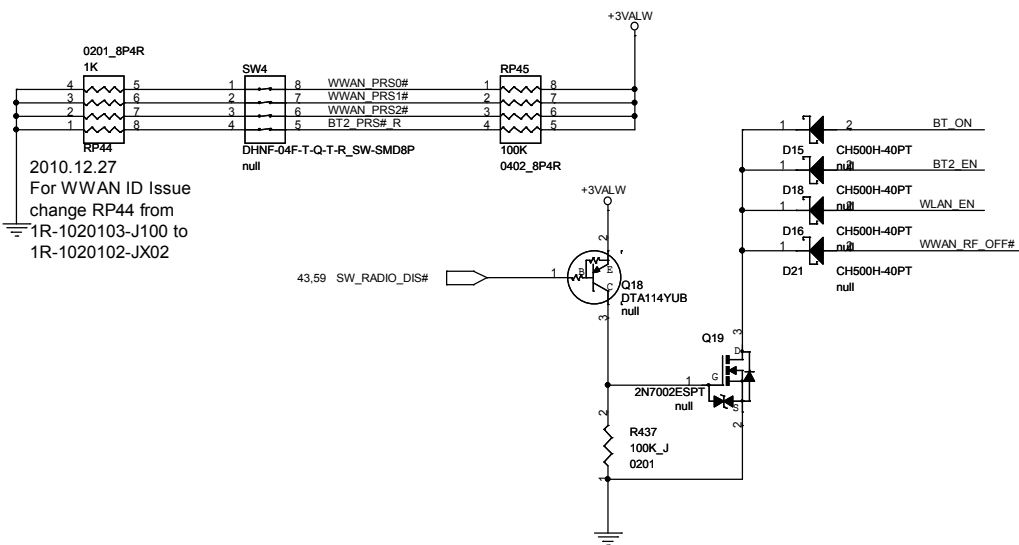
change R440 from 10K to 100K following vendor suggestion. 6/25

Remove R439 and R412 for vendor suggestion. 6/25

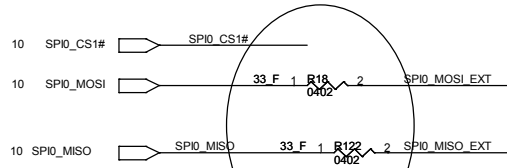
change C311and C310 to NC follow vendor suggestion 6/25



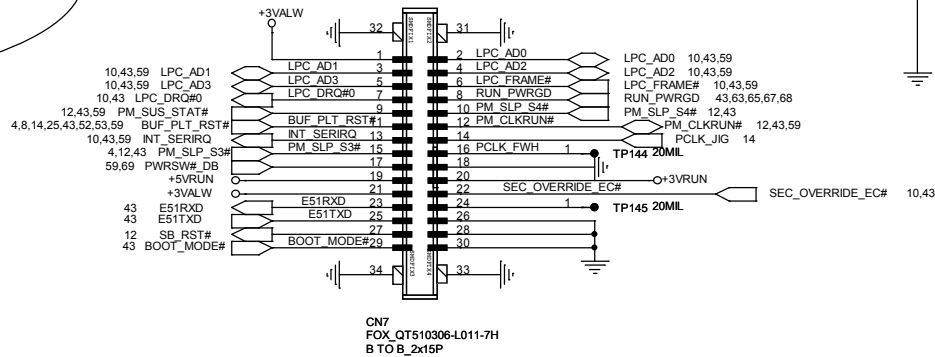
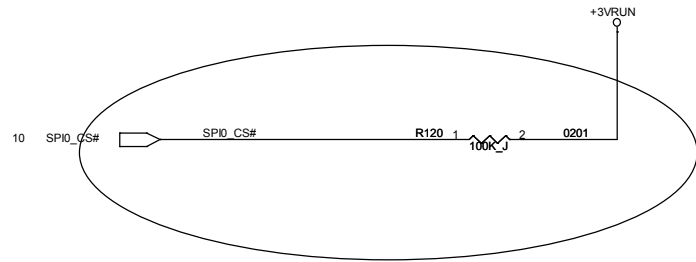
2010.12.24
For BT2_PRIS# Issue R436,R407 change from NC to munt,R441 change from munt to NC



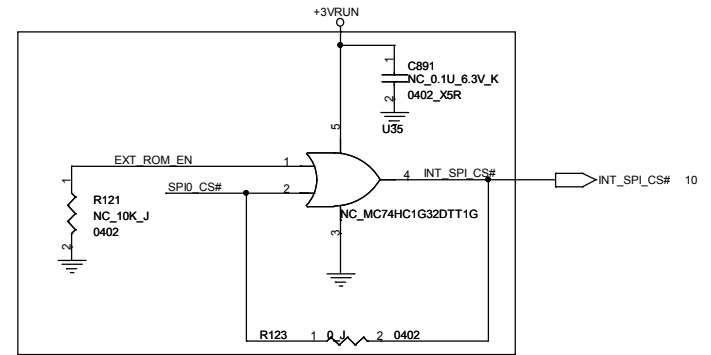
No.	Spec. of WWAN Module	WWAN_PRIS2#	WWAN_PRIS1#	WWAN_PRIS0#
0	New-A, w/ GPS	ON / Low	ON / Low	ON / Low
1	New-A, w/o GPS	ON / Low	ON / Low	OFF / High
2	New-B, w/ GPS	ON / Low	OFF / High	ON / Low
3	New-B, w/o GPS	ON / Low	OFF / High	OFF / High
4	Gobi2K, w/ GPS	OFF / High	ON / Low	ON / Low
5	Gobi2K, w/o GPS	OFF / High	ON / Low	OFF / High
6	Reserved (w/o WWAN, w/ GPS)	OFF / High	OFF / High	ON / Low
7	w/o WWAN, w/o GPS (Default setting of DIP Switch, or DIP Switch not Mounted)	OFF / High	OFF / High	OFF / High



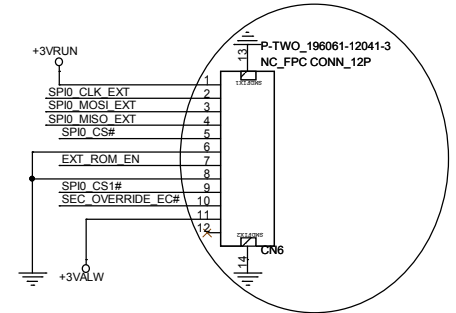
add R18 and remove R122 to P45 for debug 6/21

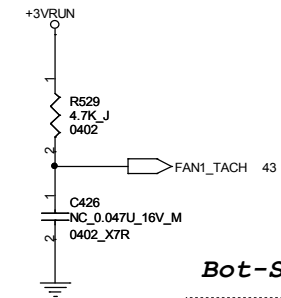
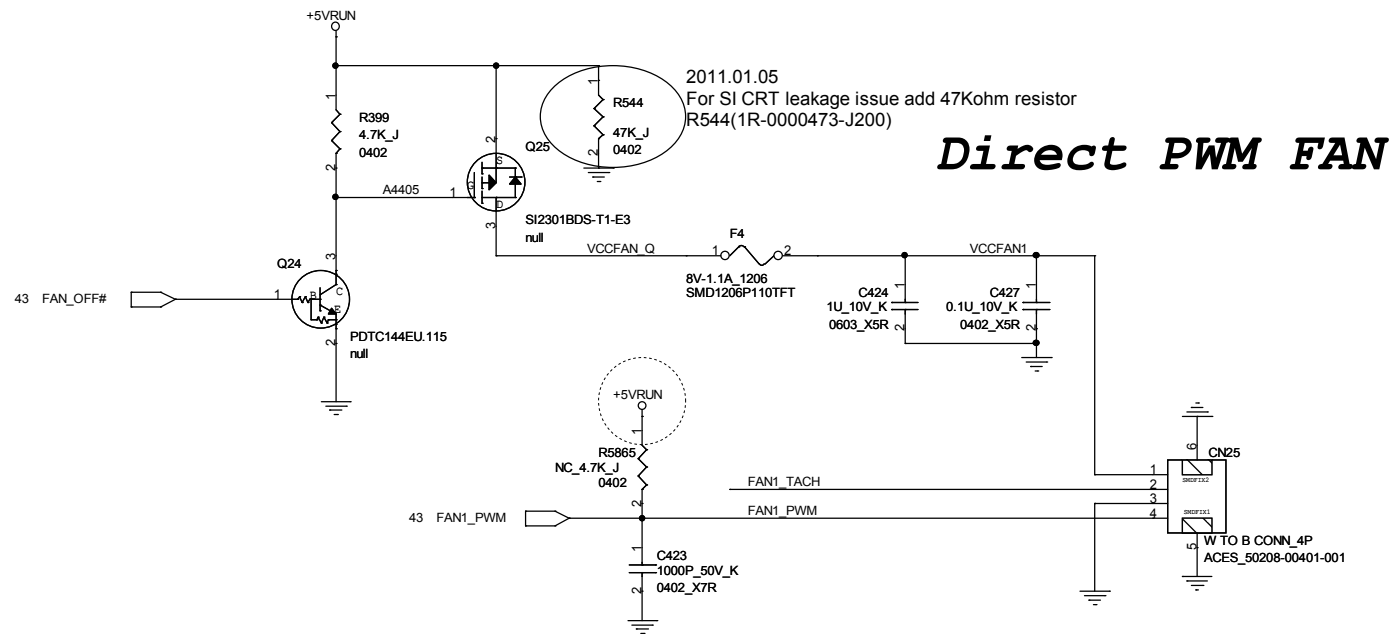


JIG-120

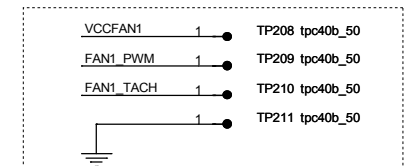


2011.1.4
For MP, change R123 to stuff and U35/R121 /C891/CN6 to NC

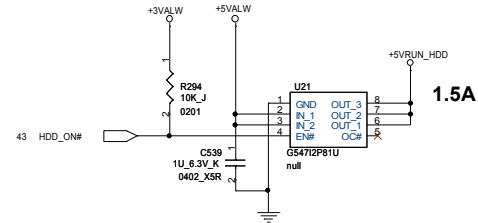




Bot-Side

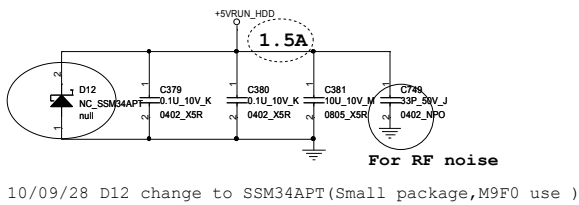
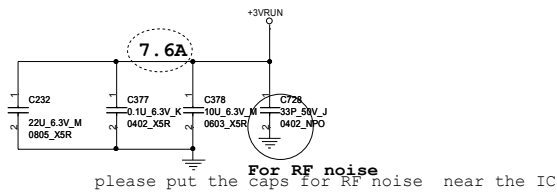


HDD Power

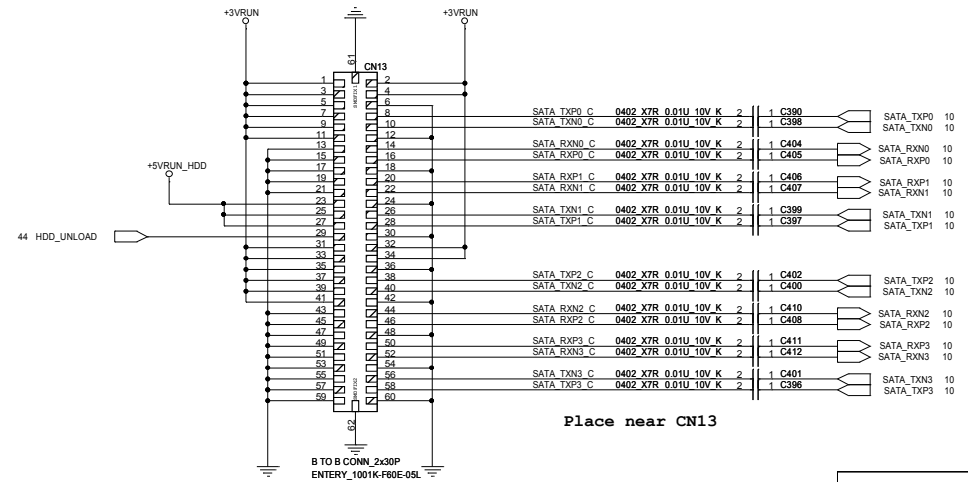


Change Power circuit for short test fail issue 10/14

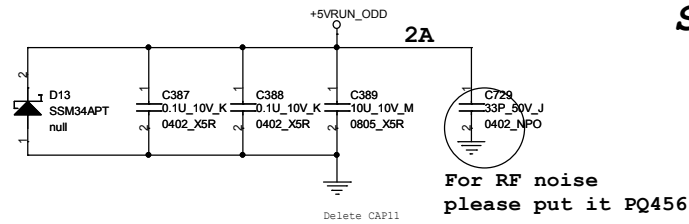
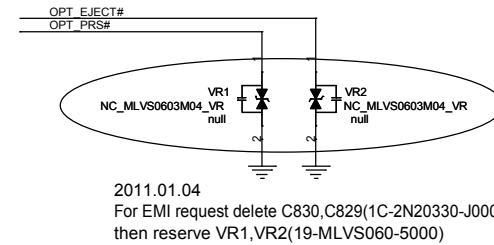
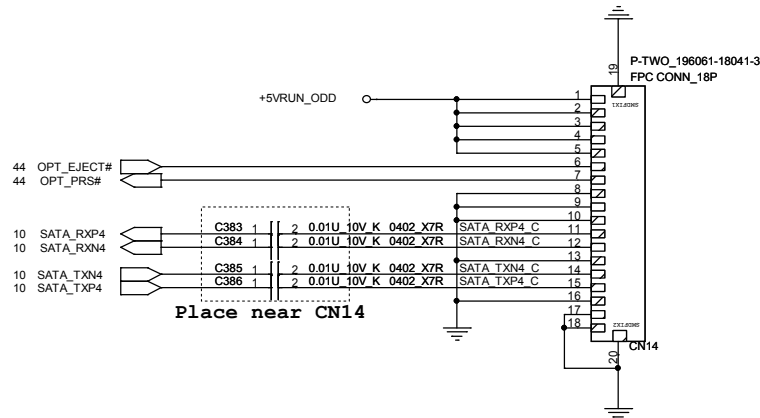
SATA HDD CONN



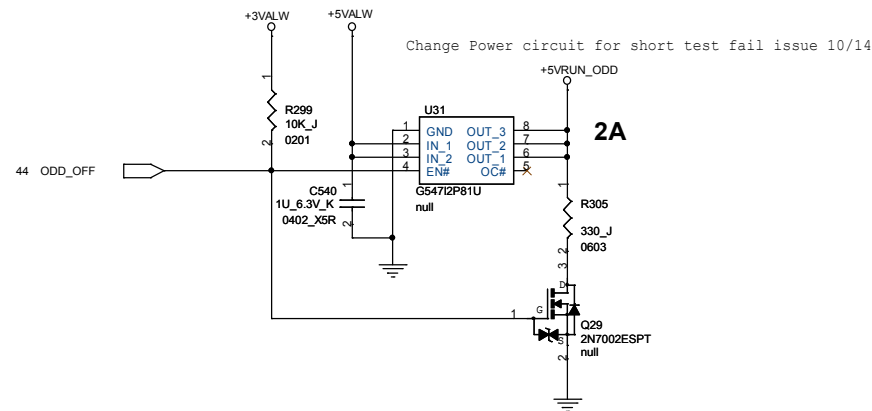
10/09/28 D12 change to SSM34APT (Small package, M9F0 use)

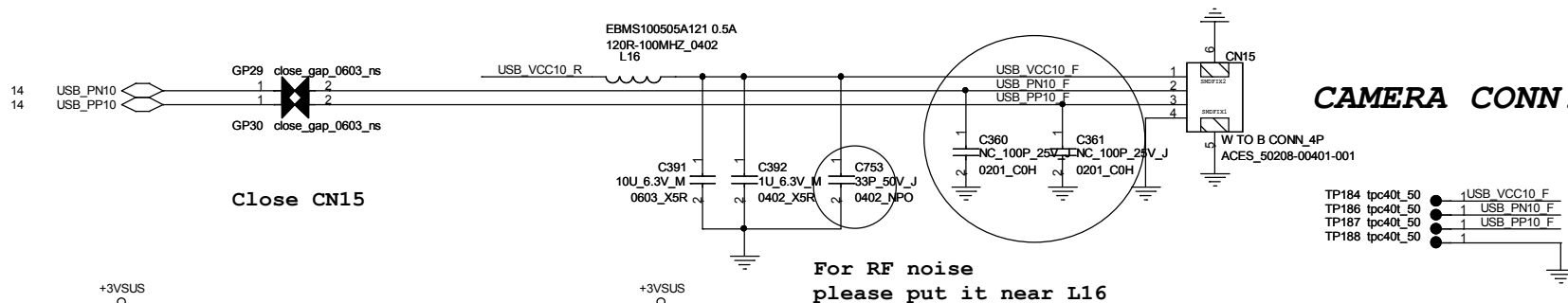


FOXCONN			HON HAI Precision Ind. Co., Ltd.
File			CCPBG - R&D Division
SATA HDD			
Size	Document Number	Rev	
Custom	V030 MP MB	1.3	
Date:	Thursday, January 20, 2011	Sheet	47 of 75



SATA ODD FPC CONN



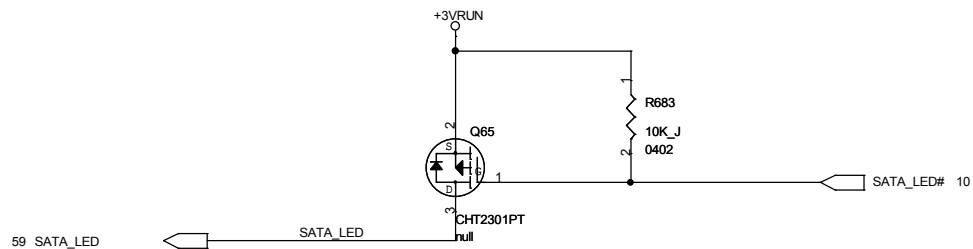


Current Limit Switch

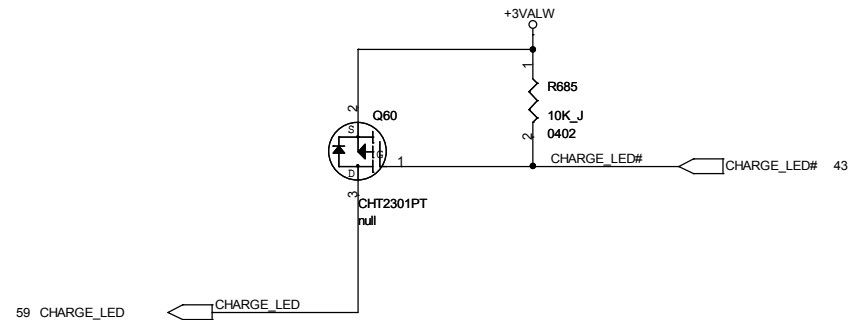
U26 co-lay with U24

$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}^{0.94}k\Omega}$$

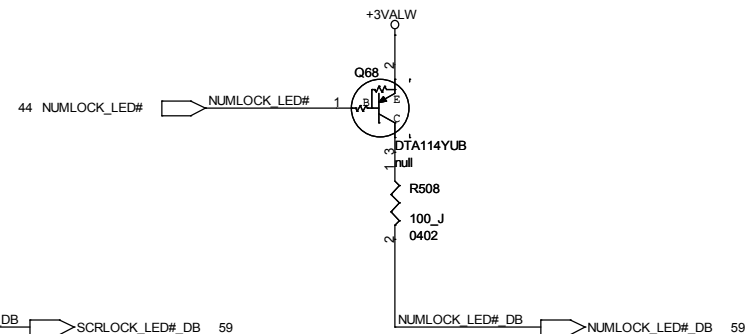
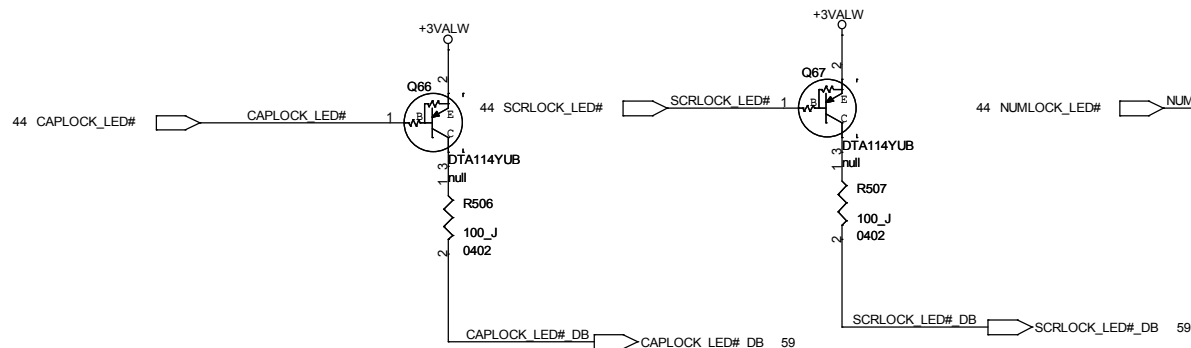
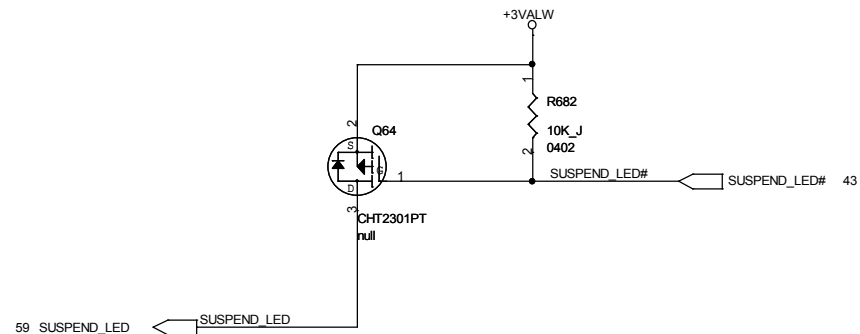
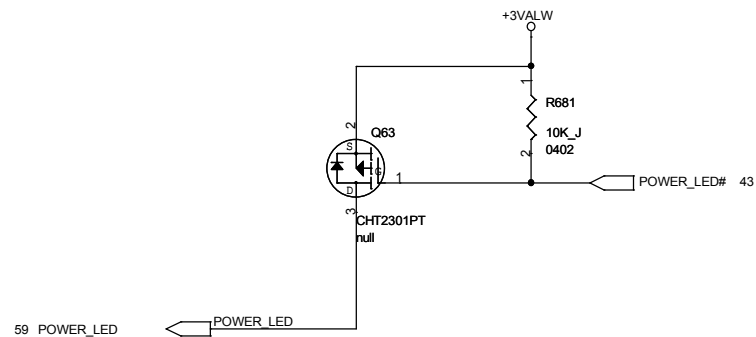
$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}^{1.016}k\Omega}$$

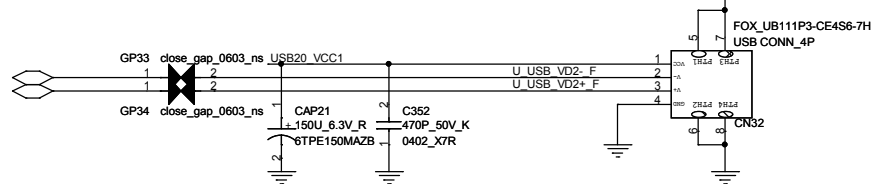
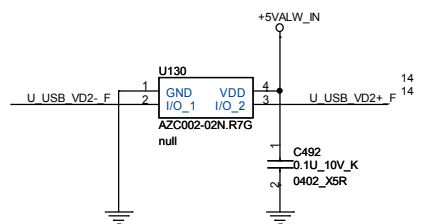
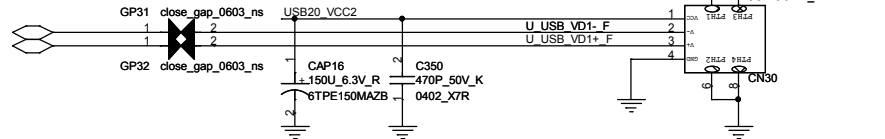
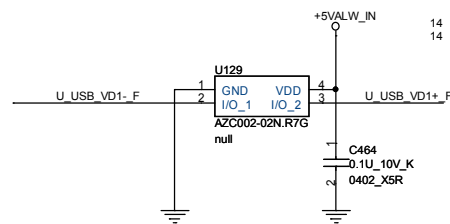
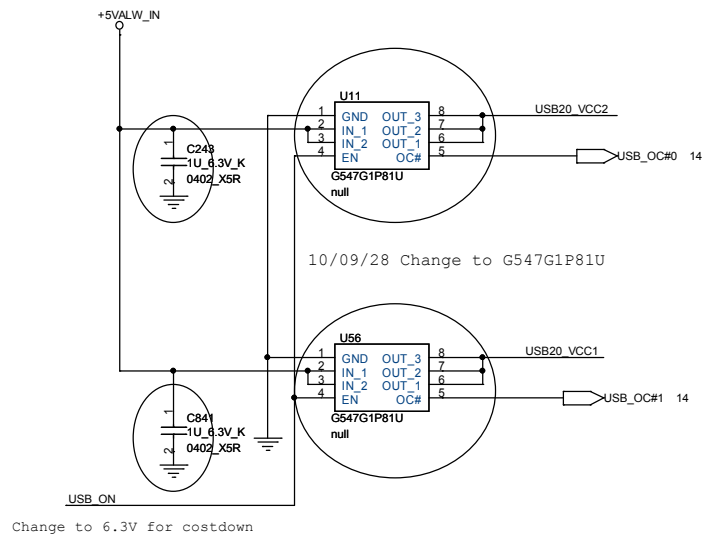
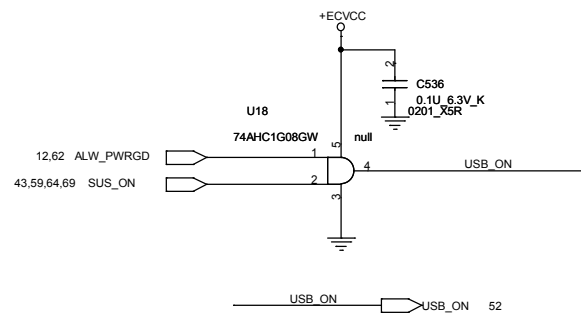


HDD/ODD LED control circuit

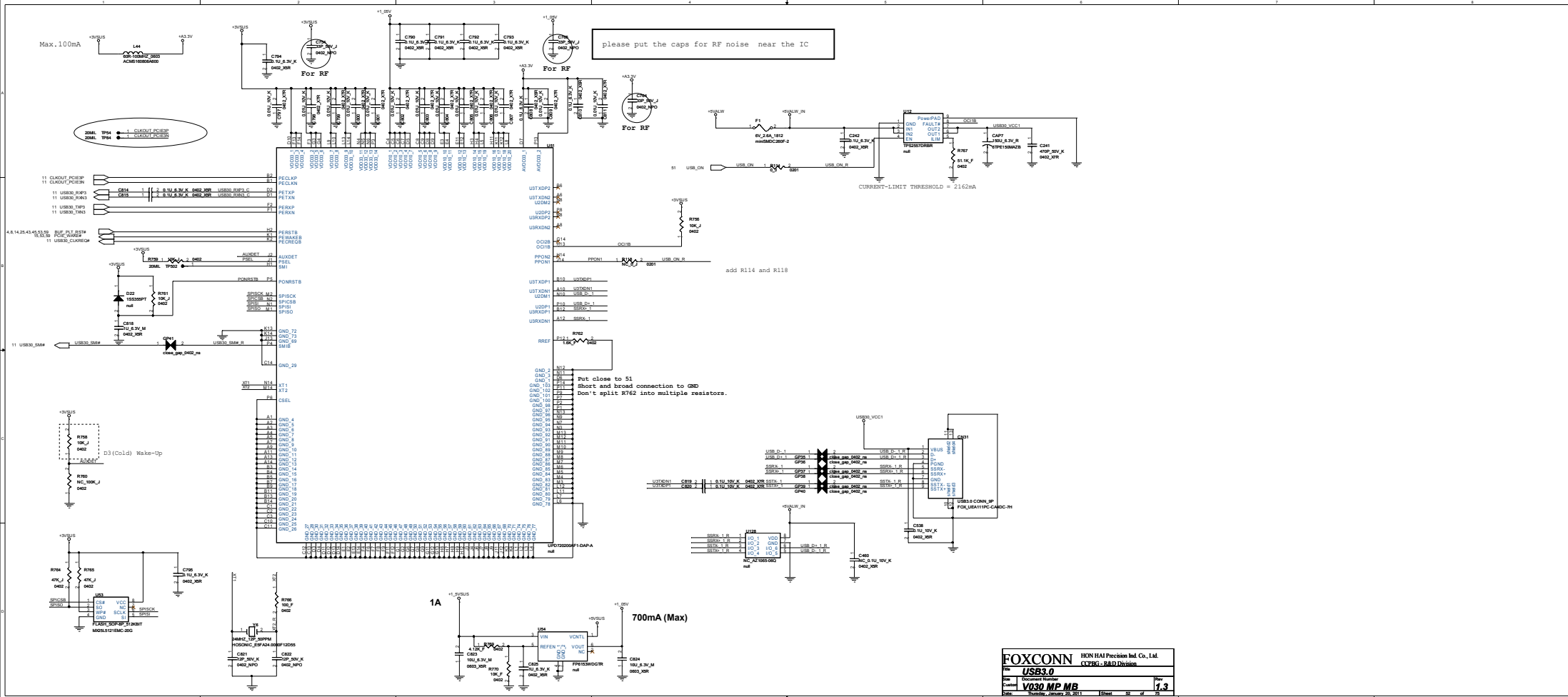


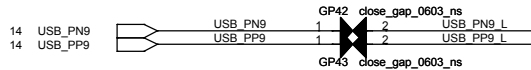
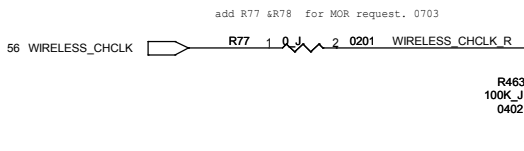
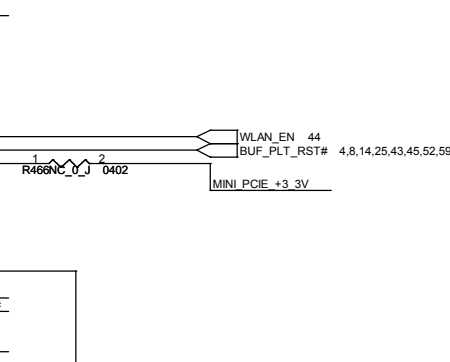
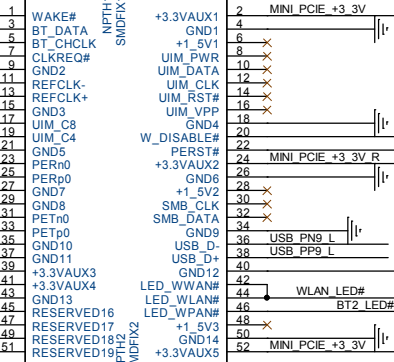
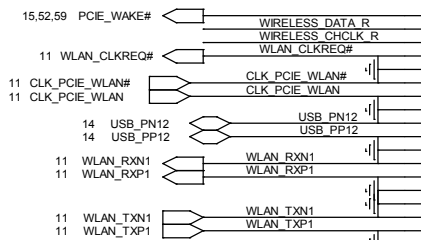
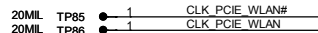
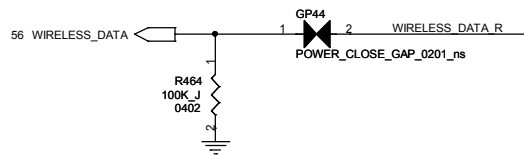
Charger LED control circuit





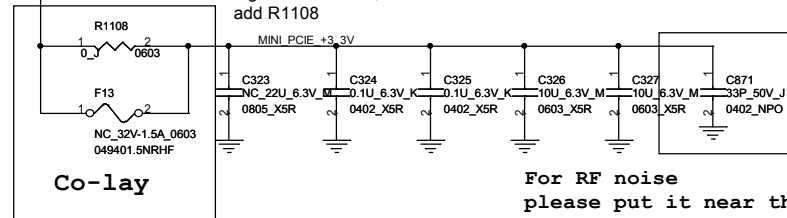
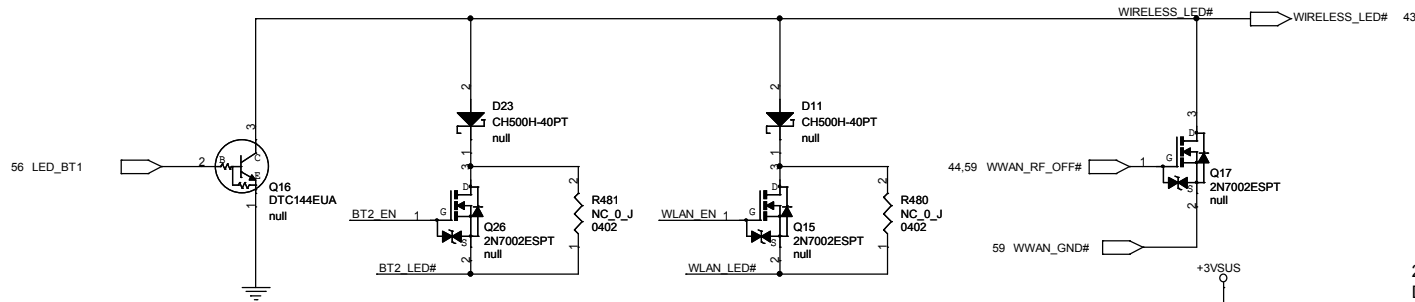
Update U129/U120 vendor PN AZC002-02N.R7G 01/20 ECR06546





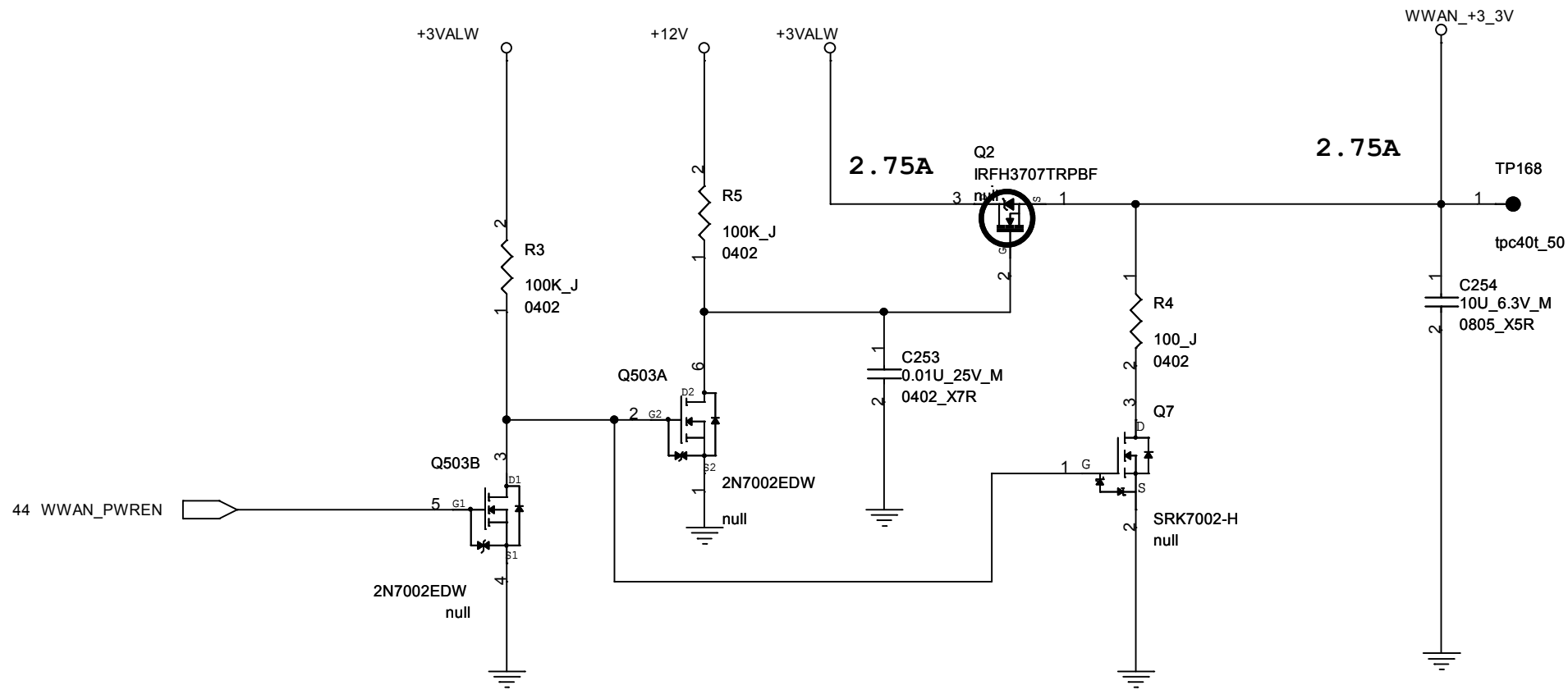
Close CN11

delete L12 for layout

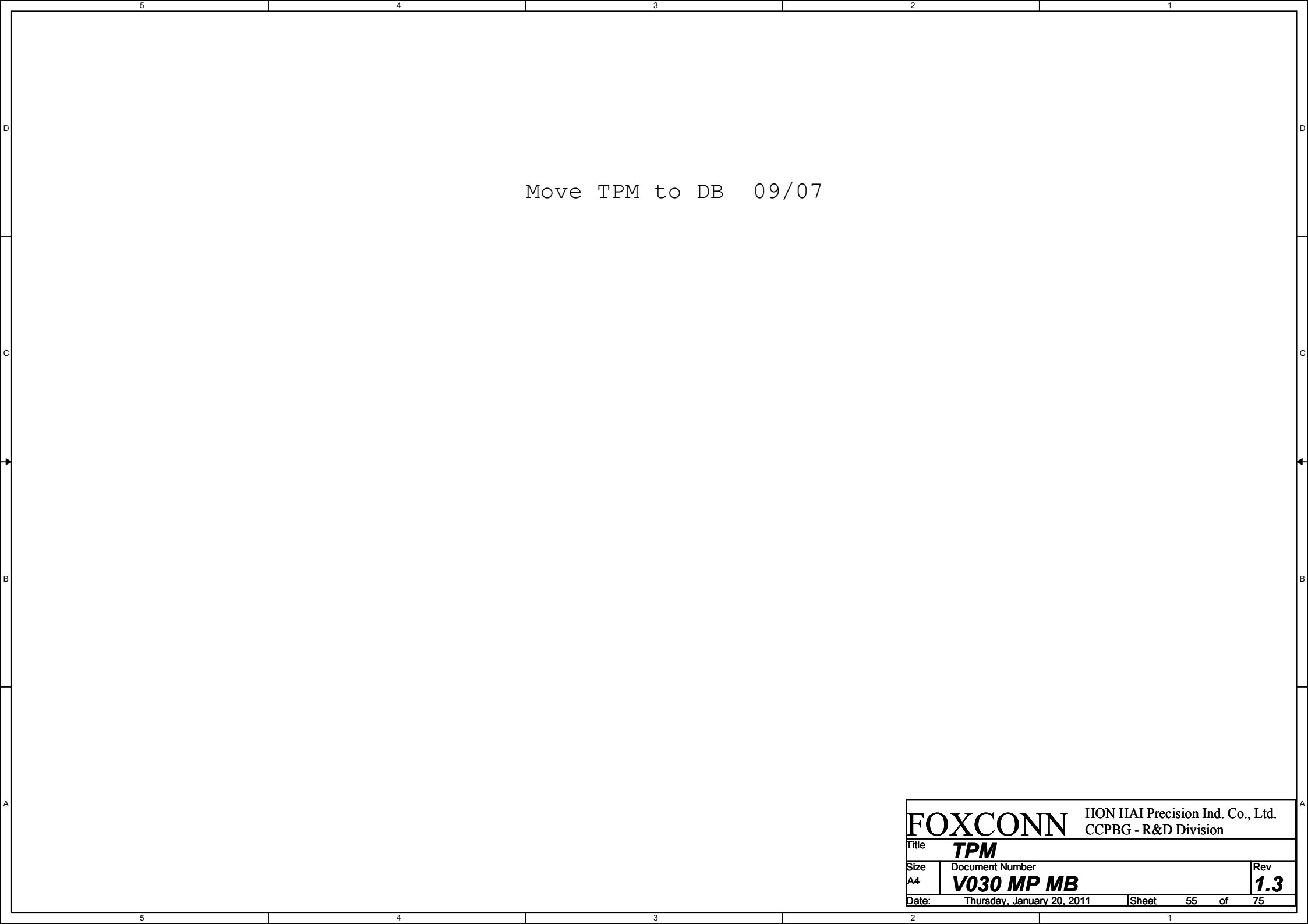


2010.1224
Due to concern of fuse voltage drop is larger than resistor, need delete F13 and add R1108

For RF noise please put it near the connector

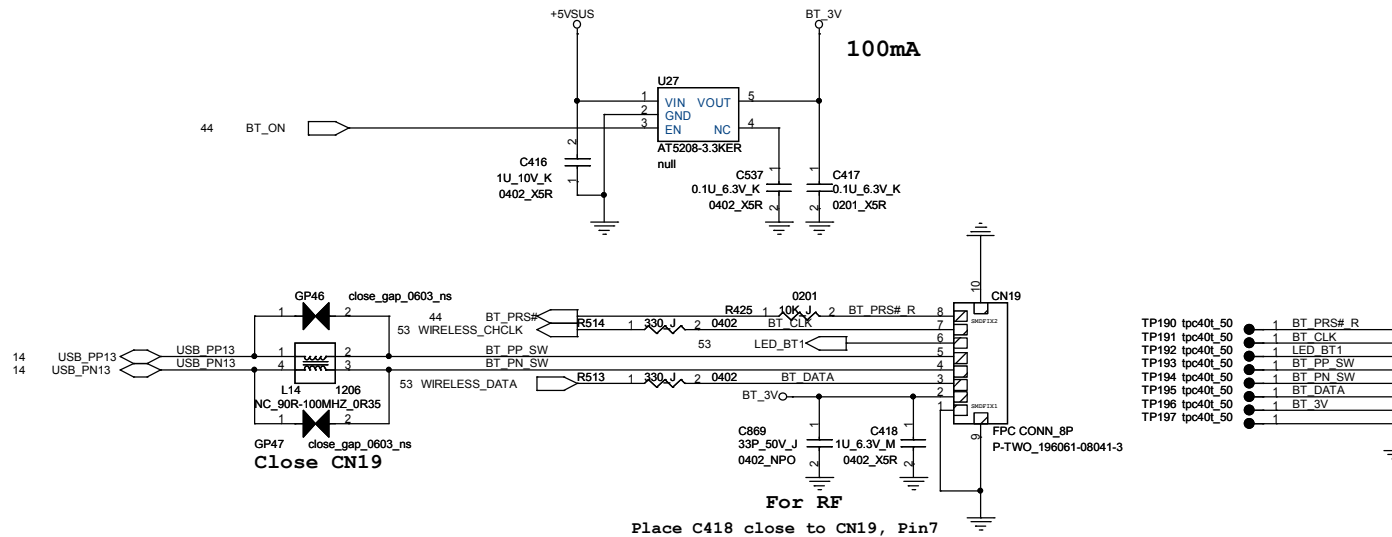


FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Mini-PCIE Card (WWAN)			
Size A	Document Number V030 MP MB		Rev 1.3
Date:	Thursday, January 20, 2011	Sheet	54 of 75

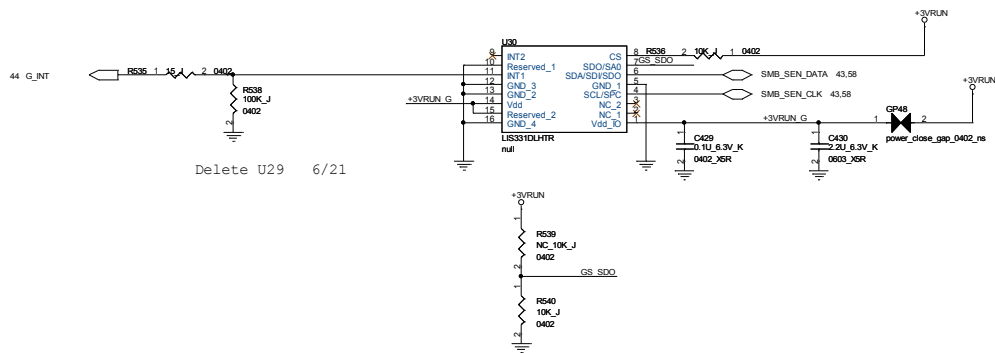


Move TPM to DB 09/07

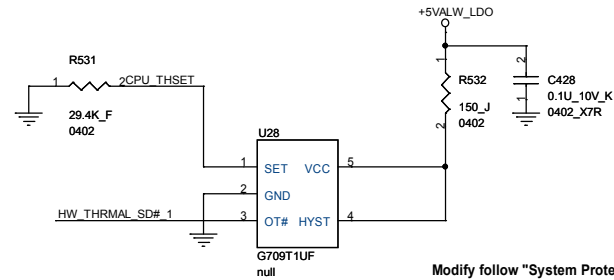
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title		TPM	
Size	Document Number		Rev
A4	V030 MP MB		1.3
Date:	Thursday, January 20, 2011	Sheet	55 of 75



Bluetooth CONN.



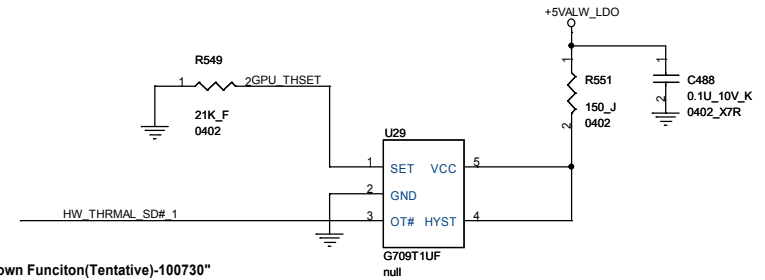
HW THERMAL PROTECTION



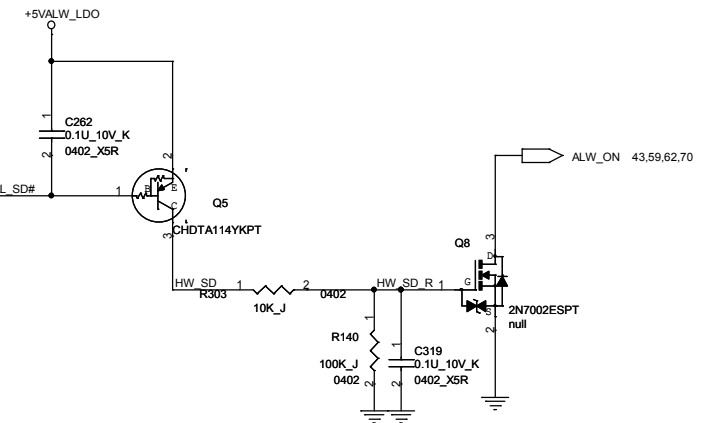
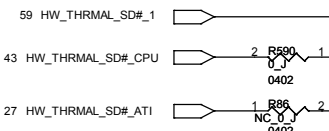
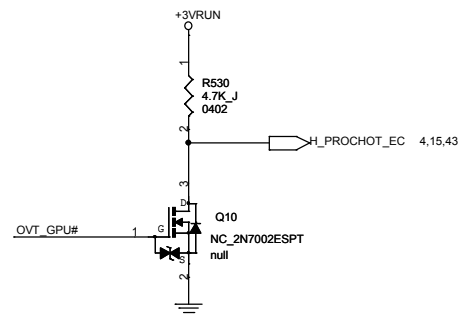
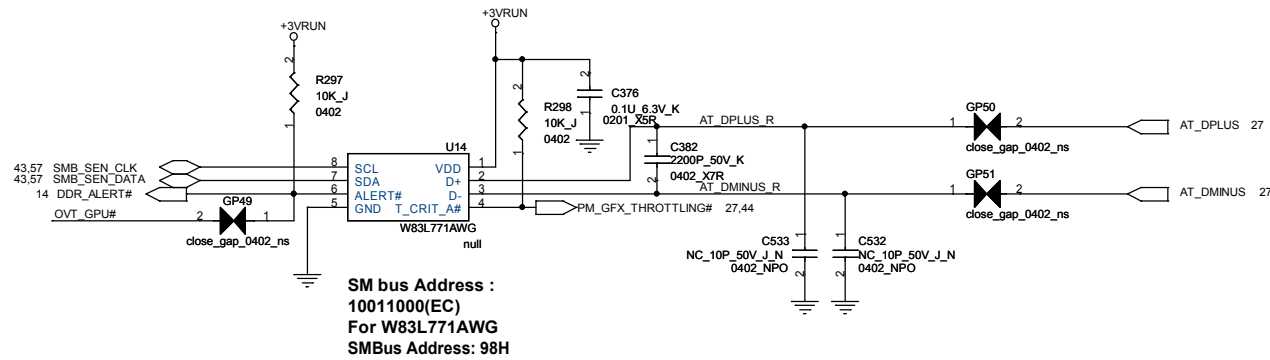
HW thermal shut down temperature setting
80 celcius degree. Put Near CPU .

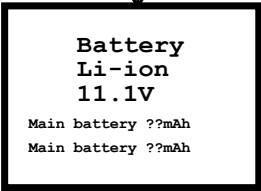
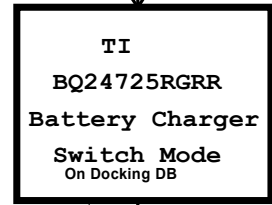
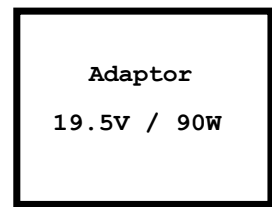
Modify follow "System Protection Shutdown Funciton(Tentative)-100730"

HW THERMAL PROTECTION

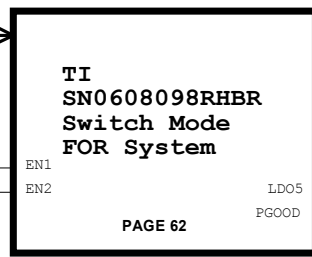


HW thermal shut down temperature setting
91.5 celcius degree. Put Near GPU .





DCBATOUT



ALW_ON

EN1

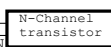
EN2

LD05

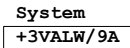
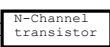
PGOOD



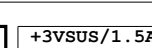
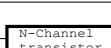
SUS_ON



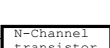
RUN_ON



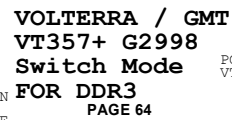
SUS_ON



RUN_ON



+5VALW



RUN_ON

SUS_ON

EN

OE

PGOOD

VTTREF

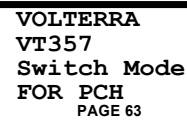


DDR3_PWRGD

DDR3_PWRGD



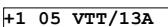
+5VALW



RUN_ON

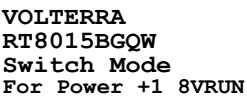
OE

PGOOD



RUN_PWRGD

+5VALW



RUN_ON

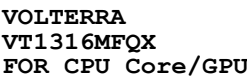
EN

PGOOD

3A

RUN_PWRGD

+5VALW



IMVP_VR_ON

VRENABLE

VRA_READY

VRB_READY

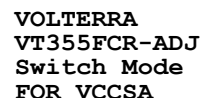
40A

20A

VHCORE/40A

+GFXCORE/20A

+5VALW



RUN_PWRGD

EN/PSV

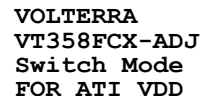
PGOOD

4A

RUN_PWRGD

VCCSA/4A

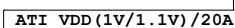
+5VALW



PEG_PWR_OFF#

EN/PSV

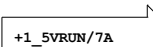
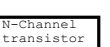
PGOOD



RUN_PWRGD

BQ24725_VCC_R

RUN_ON1

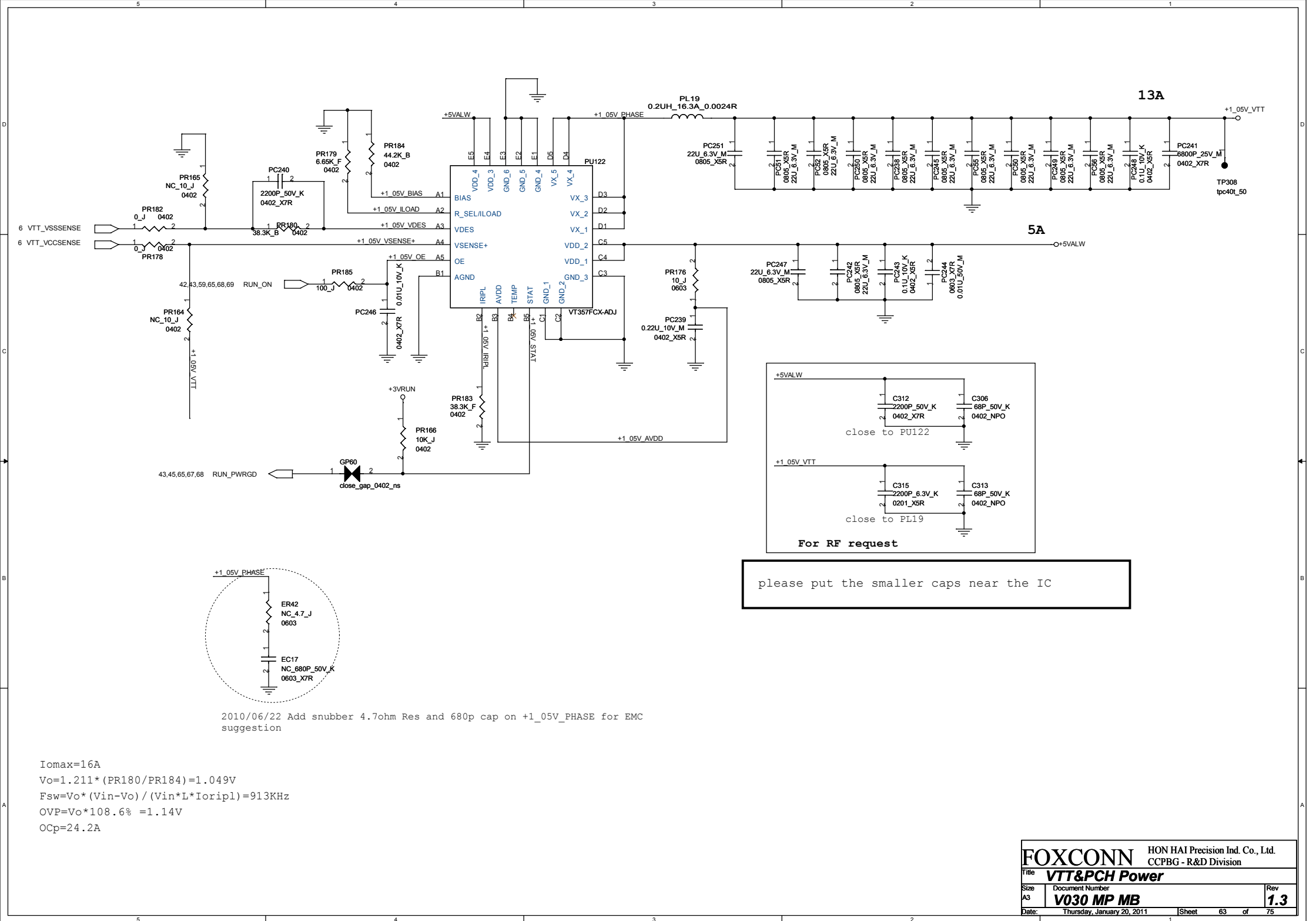


+1_5VSUS



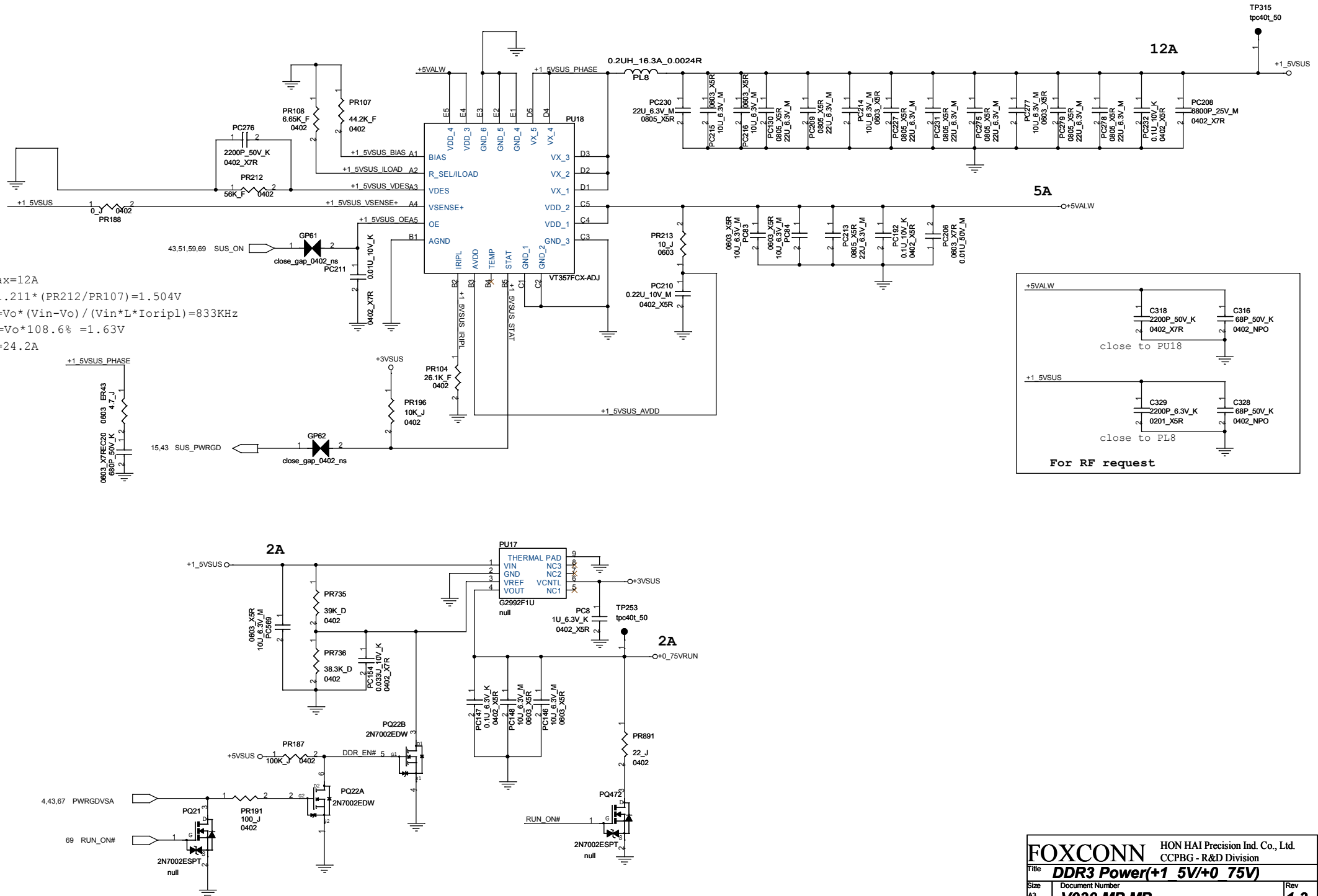
PEX_VDD/2.5A

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	Power Design Diagram		
Size	Document Number	Rev	
Custom	V030 MP MB	1.3	
Date:	Thursday, January 20, 2011	Sheet	60 of 75

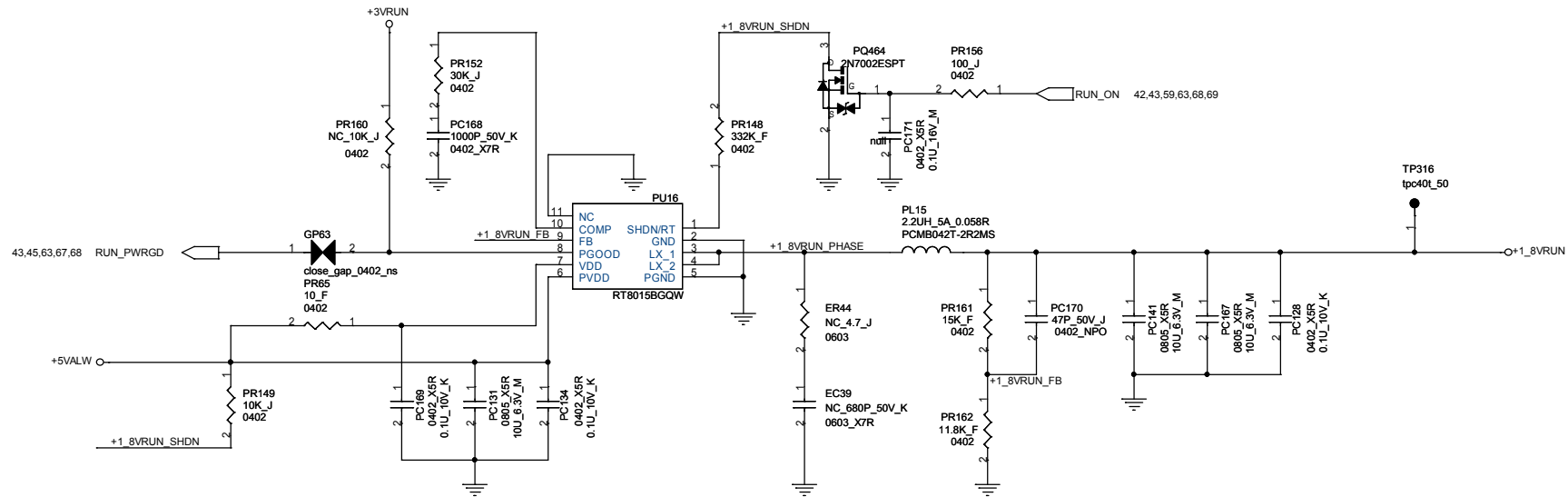


$I_{omax}=16A$
 $V_o=1.211 \times (PR180/PR184)=1.049V$
 $F_{sw}=V_o \times (V_{in}-V_o) / (V_{in} \times L \times I_{orip1})=913KHz$
 $OVP=V_o \times 108.6\% =1.14V$
 $OCp=24.2A$

$I_{\text{omax}}=12\text{A}$
 $V_o=1.211 \times (\text{PR212}/\text{PR107})=1.504\text{V}$
 $\text{Fsw}=V_o \times (\text{Vin}-V_o) / (\text{Vin} \times L \times I_{\text{oripl}})=833\text{KHz}$
 $\text{OVP}=V_o \times 108.6\% =1.63\text{V}$
 $\text{OCp}=24.2\text{A}$

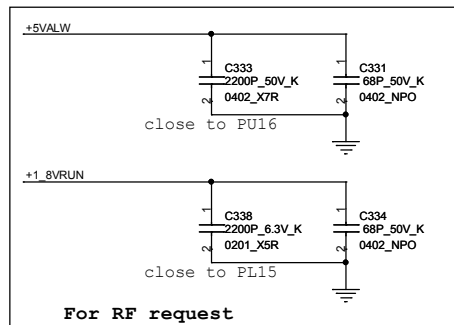


10/05/18 Change 1_8VRUN power IC from LDO IC OZ8033GN back to VT355 for efficiency considerable.
 10/05/21 Change PR162 from 43K to 9.1K.
 10/09/17 Change +1_8VRUN IC from VT355 to RT8015BGQW

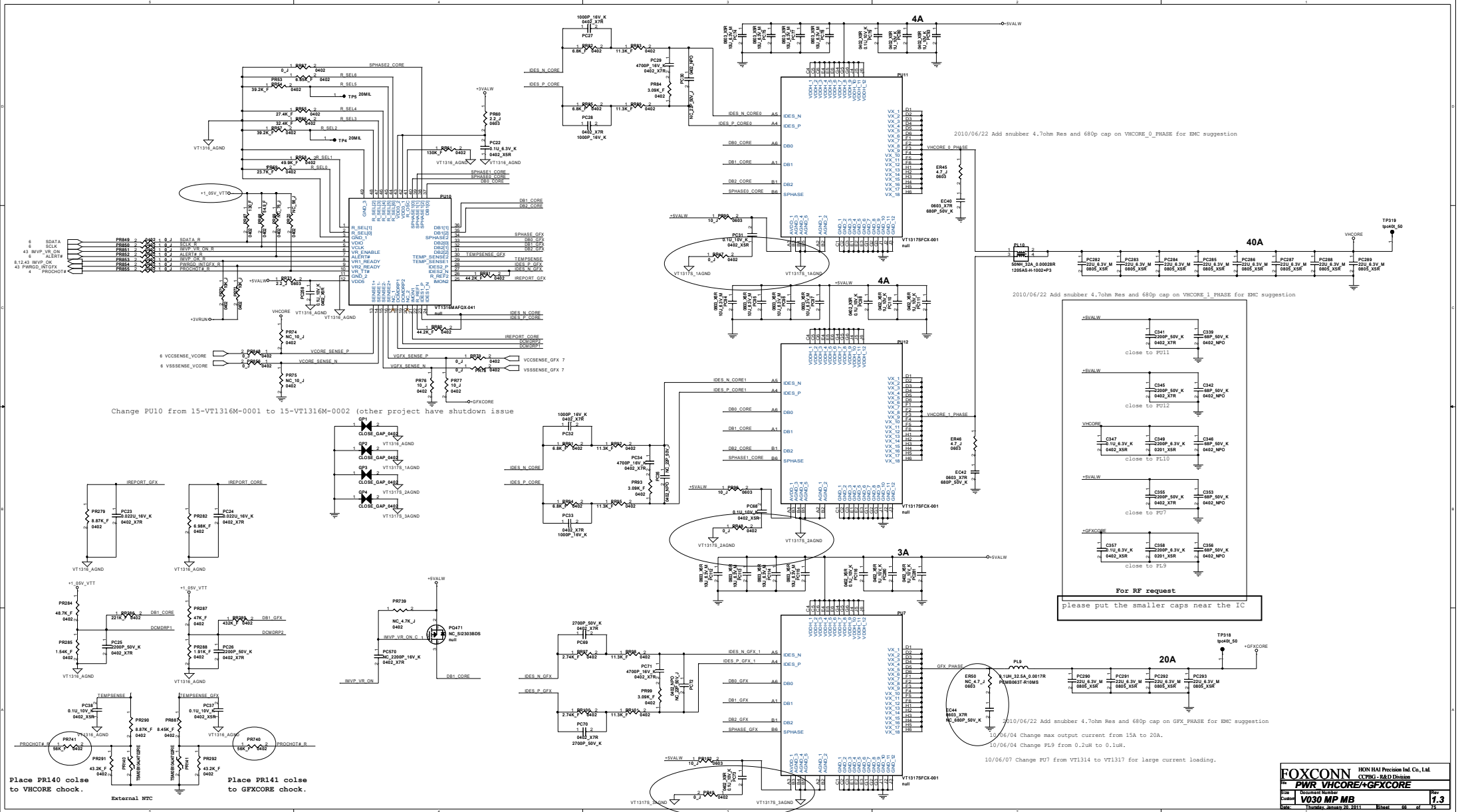


OCP = 3.8A
 Fsw = 1000KHz
 $V_o = (1 + (PR87/PR89)) * 0.8 = 1.8169V$
 OVP => VFB * 112.5%
 UVP => VFB * 75%

please put the smaller caps near the IC

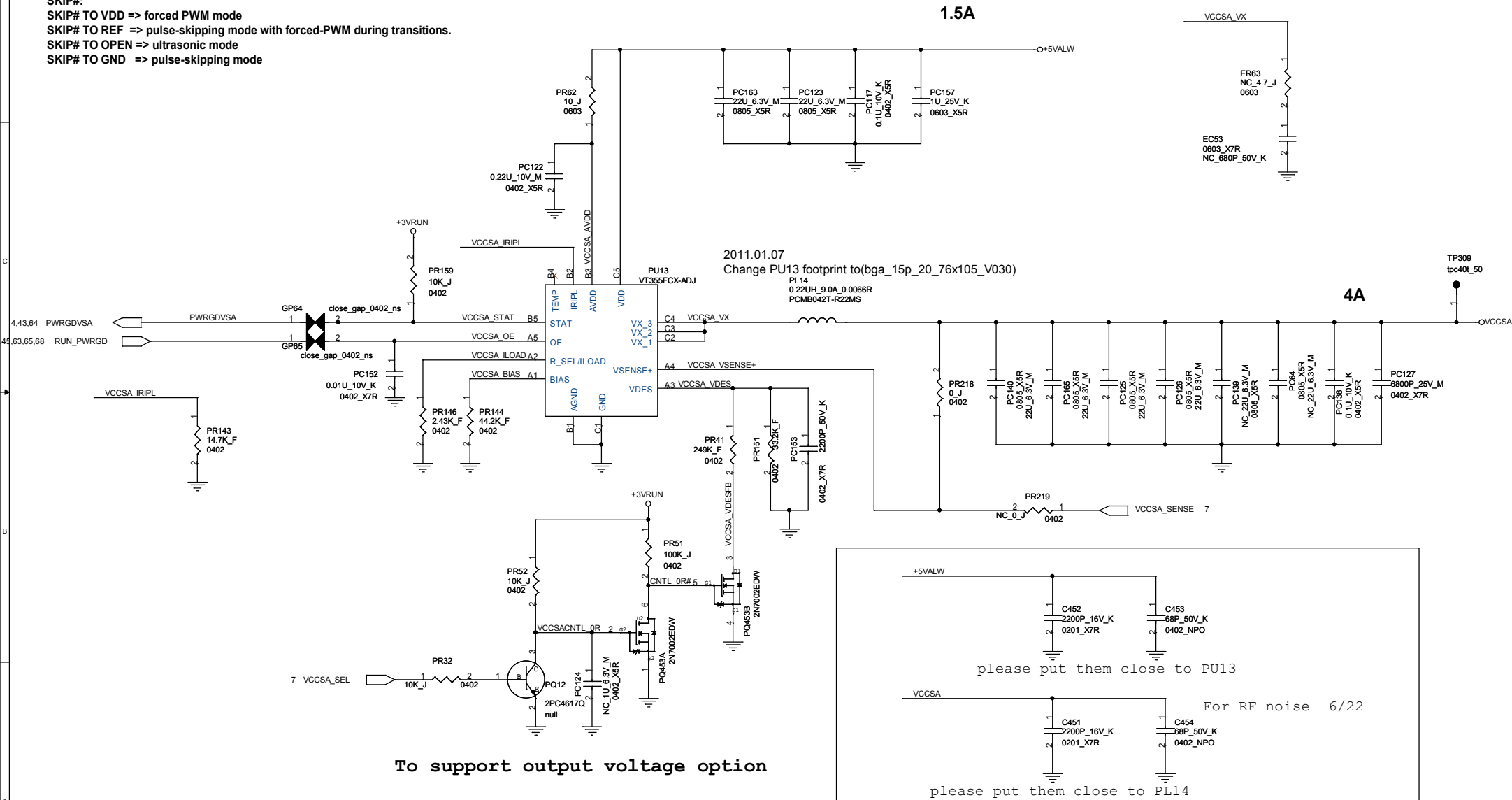


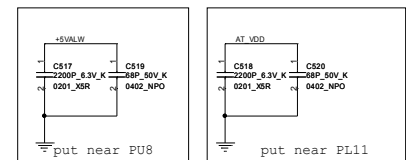
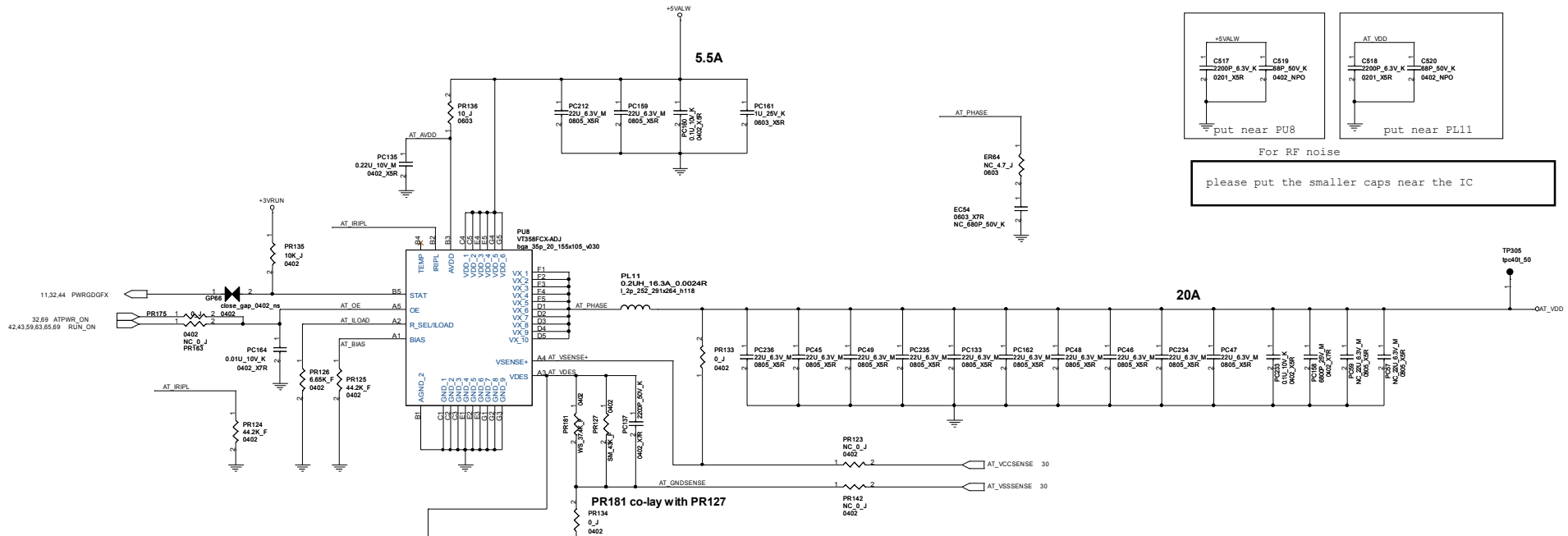
For RF request



$I_{omax}=4A$
 $V_o=1.211*(PR151/PR144)=0.9096V$
 $V_o=1.211*((PR41*PR151)/(PR41+PR151)*PR144)}=0.811V$
 $F_{sw}=V_o*(V_{in}-V_o)/(V_{in}*L*I_{oripl})=877KHz$
 $OVP=V_o*108.6\%=1.01V$
 $OCP=8.1A$

SKIP#:
SKIP# TO VDD => forced PWM mode
SKIP# TO REF => pulse-skipping mode with forced-PWM during transitions.
SKIP# TO OPEN => ultrasonic mode
SKIP# TO GND => pulse-skipping mode





For RF noise
please put the smaller caps near the IC

2010.1224
Our current AT_VDD is not meet AMD the min spec
Change PR118 From 1R-0000334-F200 to 1R-0000474-J200
PR118 co-lay with PR113

2010.1227
For V30 MP PR118 change
from 5%(1R-0000474-J200)
to 0.5%(1R-0004703-D200)
PR181 co-lay with PR127

Whistler LP is
(EngineCLK:500Mhz MemCLK:800Mhz)

Seymour XT is
(EngineCLK:750Mhz MemCLK:900Mhz)

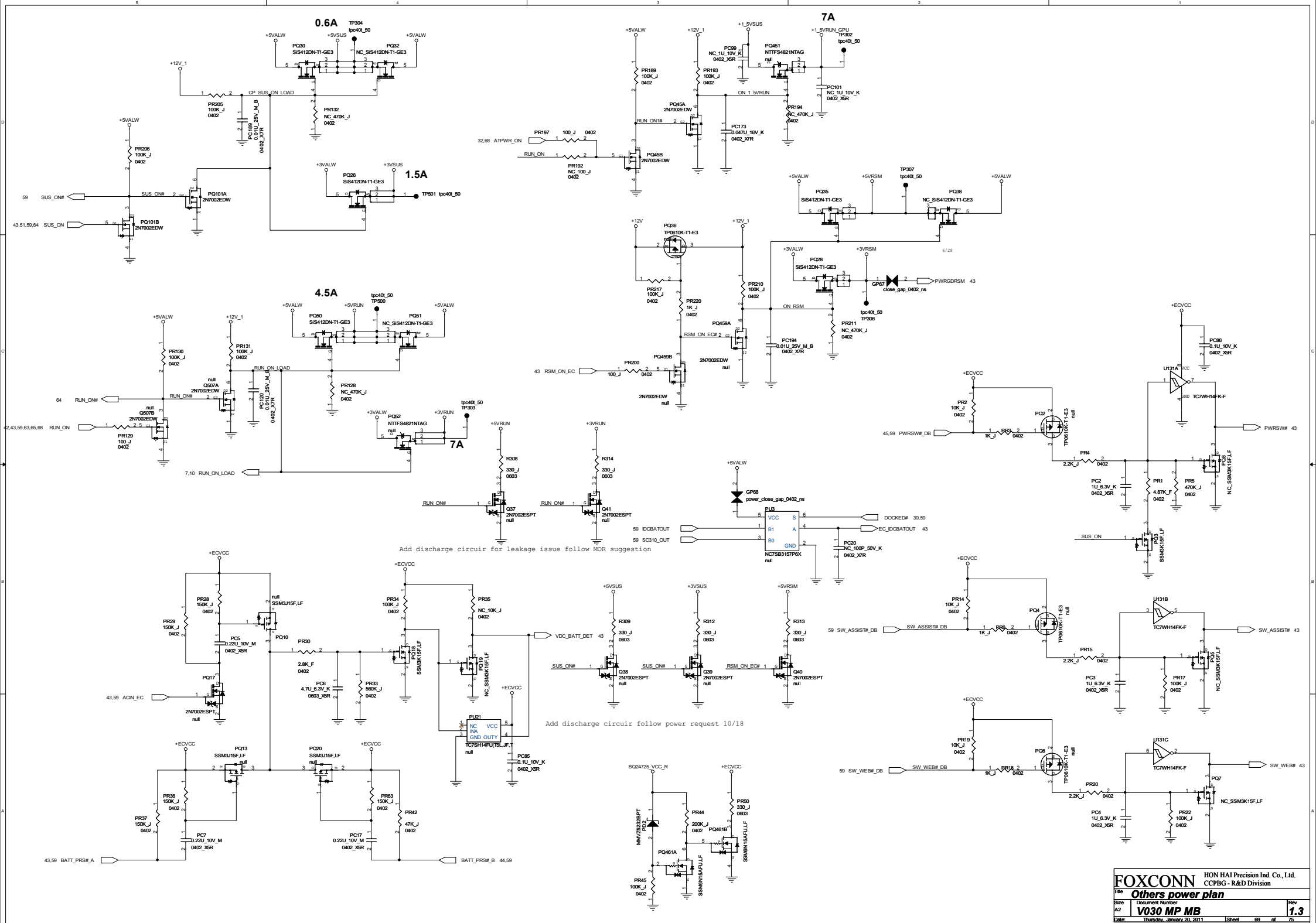
Whistler-LP M2 VCore PWRCTRL_1 define as
0: 1.0V, 1: 0.90V
Seymour-XTX M2 VCore PWRCTRL_1 define as
0: 1.15V, 1: 0.90V

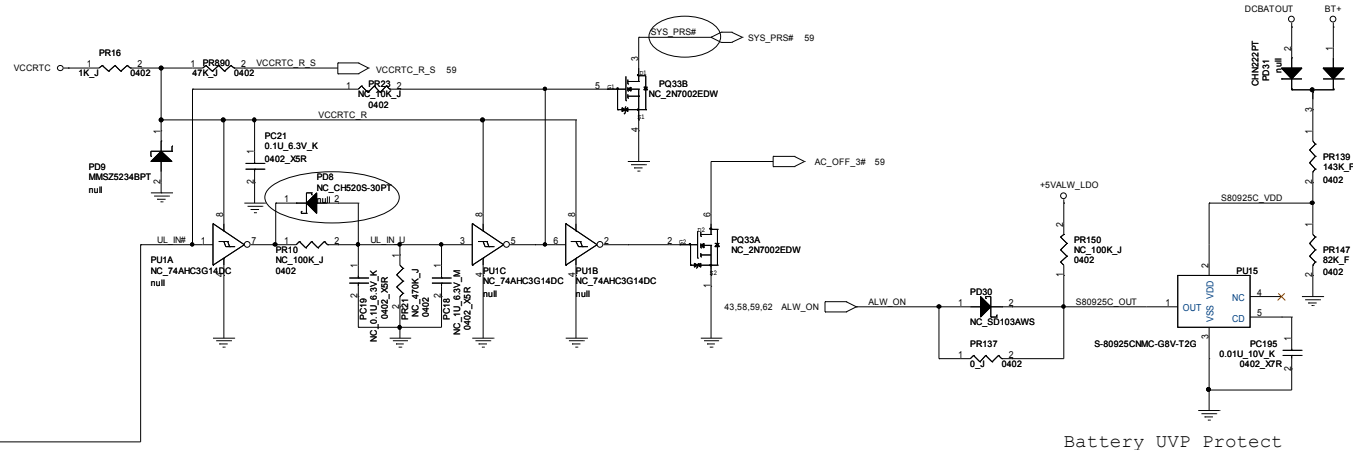
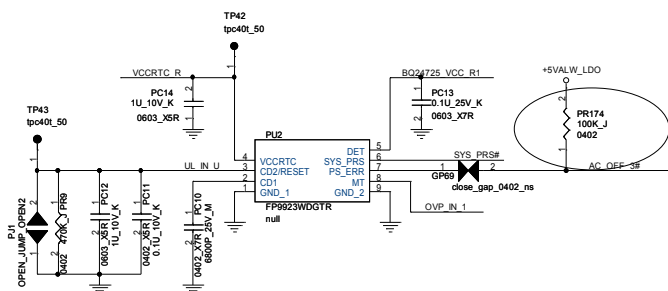
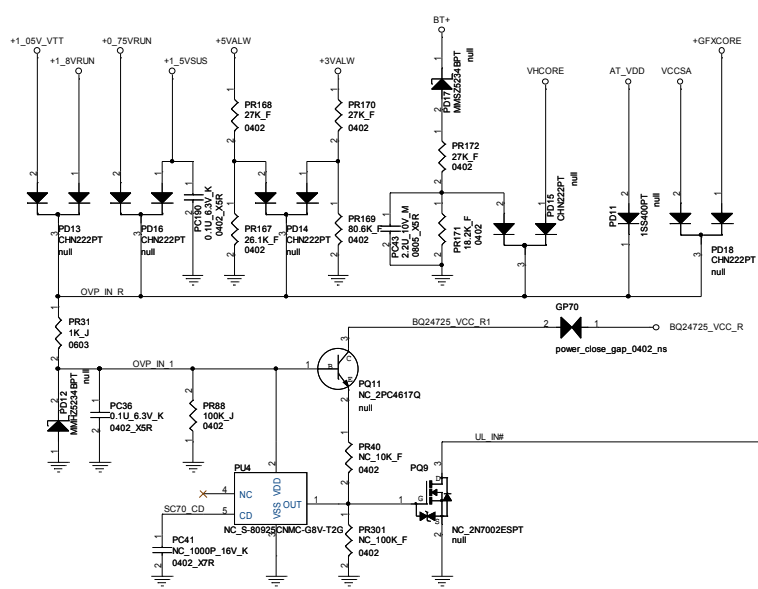
SKIP#:
SKIP# TO VDD => forced PWM mode
SKIP# TO REF => pulse-skipping mode with forced-PWM during transitions.
SKIP# TO OPEN => ultrasonic mode
SKIP# TO GND => pulse-skipping mode

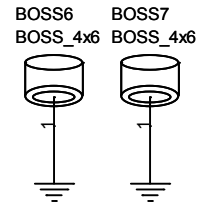
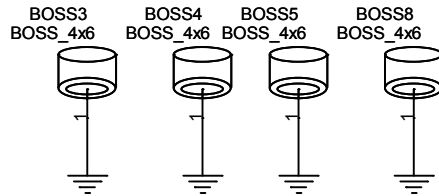
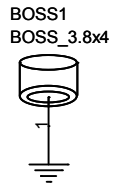
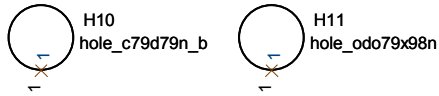
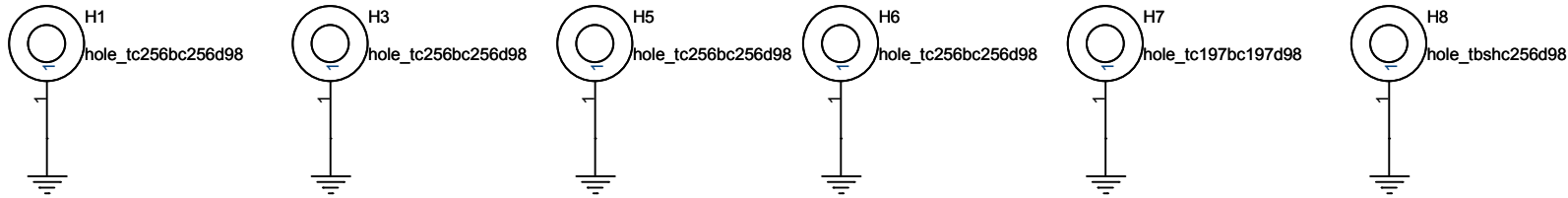
Iomax=24A
Vo=1.211*(PR127/PR125)=1.1288V
Vo=1.211*{ (PR127*PR113)/[(PR127+PR113)*PR125] }=0.903V
Fsw=Vo*(Vin-Vo)/(Vin*L*Iorip1)=851.8KHz
OVP=Vo*108.6% =1.23V
OCP=32.2A

Change PR222 from 3.3K to 2.8K to set PEX_VDD voltage from 1.05V to 1.02V.

$$V_o = (1 + (PR222/PR229)) * 0.8 = 1.02V$$







WLAN Module

Thermal Modul

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Size	Document Number		Rev
	V030 MP MB		1.3
Date:		Thursday, January 20, 2011	Sheet 71 of 75

7/29
[15 -- PCH (GPIO,VSS_NCTF,RSVD)] delete R262 for dupliacate pull-up for PCIE_WAKE_F
[39 -- CRT] add R913,R914 and R915 for no docking sku
7/31
19~24 Change cap from 0402 size to 0201 size
08/02
[64 -- DDR3 Power(+1_5V/+0_75V)] PC214&PC277 change to 4pcs 10u (PC214/PC277/PC215/PC216)
08/03
[71 -- Hole & BOSS & AMI LABEL] Change BOSS4 to H40M20-15351028P1D4BM
[52 -- USB 3.0] Change U53 to MX25L5121EMC-20G and NC R771
08/04
[58 -- H/W Thermal Protect]Separate nets of U28.1 &U29.1

08/09
[42 -- HDMI] Swap TMD5_TX2 with TDS_TX0
[48 -- SATA ODD] Combine PQ463&PQ458 to 2in1 package
[55 -- TPM] Add R151,R152,R153,R154
08/10
[49 -- Camera] CN15 change to ACES_88460-0401
[56 -- Bluetooth Connector] CN19 change to P-TWO_196061-08021-3
[26 -- ATI VGA (Strap)] Update strap table
[66 -- CPU Power_VHCORE]Change PR54 from 1R-0002742-F200 to 1R-0003922-F200 follow Intel suggestion
[54 -- Mini-PCIE Card(WWAN) Q7 Change to 17-SRK7002-H000 (HF)
[04 -- SNB (CLK,MISC,JTAG)] U2/U3 change to 14-SN74LVC-1G1H

08/11
[42 -- HDMI] R552/R553/R554/R555/R556/R557/R558/R559 change to 0402 size
08/16
P.13 {PCH (LVDS,DDI)} Modify HDMI signal data0/2(+/-) to data5/3(+/-) for the PR function.
P.43 {EC} Move C219 to colse U16 from MOR suggestion.
P.59 {MB to DB} Delete D24, Because for the DB already have L_D1, So can delete.
P.71{BOSS} Delete H2 from ME suggestion.
P.32{ATI VGA (GND)} Q190/Q191/Q192/Q193 change to BSR202N follow MOR requirement

08/17
[59 -- MB to DB Conn] CN35 /CN37 change to KOTL_F32250-H11101
[59 -- MB to DB Conn] CN37 Pin 22 change to +5VALW_LDO [For thermal sensor on DB]
[59 -- MB to DB Conn] CN37 Pin 20 change to HW_THRMAL_SD#_1[For thermal sensor on DB]
[58 -- H/W Thermal Protect] C319 change to X5R
[56 -- Bluetooth Connector] C417 change to X5R
[46 -- FAN] C427 change to X5R
[41 -- Inverter] C434/C448 change to X5R
[61 -- Identify IC] PC320 change to X5R
[54 -- Mini-PCIE Card (WWAN)] Q503 change to 2N7002EDW for PUR suggestion
[32 -- ATI VGA (GND) 8/8] Q496 change to 2N7002EDW for PUR suggestion
[58 -- H/W Thermal Protect] Add R530/Q10 for level shift

08/18
[15 -- PCH (GPIO,VSS_NCTF,RSVD)] Add R327/R336. Reserve D4/D5
[10 -- PCH (HDA,JTAG,SAT)] Delete R133/R134/R136.
[10 -- PCH (HDA,JTAG,SAT)] R117 change to 4.7K follow intel spec
[04 -- SNB (CLK,MISC,JTAG)] U25 change to 74AHC1G09GW. Delete C33/U2
[04 -- SNB (CLK,MISC,JTAG)] Delete H_SNB_IVB# follow intel spec
[14 -- PCH (PCI,USB,NVRAM)] Delete R238 ,R237 change to 2.2K follow intel spec

08/19
[59 -- MB to DB Conn] Delete CN12
[43 -- EC + SPI ROM] Change RP19 to R133/R134 (Power request pull high 2.2K)
[70 -- OVP protection] Change PC13 from Y5V to X7R
[66 -- CPU Power_VHCORE] Change PR82/RP85/PR91/PR94 from 7.32K to 4.3K
[66 -- CPU Power_VHCORE] Change PR97/PR100 from 3.4K to 2.74k
[69 -- Others power plane] Change PC5/PC7/PC17 from 0.1uF to 0.22uF
[69 -- Others power plane] Change PR30 from 2.2K_J to 5.6K_F
[62 -- SYS Power (+3_3V/+5V)] Delete PR11/PR12 (PR120/PR118 have same function)
[70 -- OVP protection] Delete PR187/PR174/PR181/PR186/PR190/PR191/PC42/PC40/PC1/PC44/PC39/
PD1/PU5/PQ464/PQ1

08/20
[P44&P53]Change WLAN_EN# to WLAN_EN
[59 -- MB to DB Conn.] Exchange U20 pin2 with pin4 (Wrong connection)
[P19-P23] Delete 376,1000,1004,1008,1012,1016,1020,1024,1028,1032,1036,1040,1044,1048,1052,1056,1060. (Short 0 ohm)
[40 -- LVDS] Change CN26 to FOX_GS03407-1113A-7H
[43 -- EC + SPI ROM] Change Y4 to EPSON_MC-146
[51 -- USB 2.0] U11/U56 change to FP6861B-B1MSGTR

08/20
[70 -- OVP protection]Delete PR120/PR118/PR109/PR86/PQ21/PR39/PC8/PR111/PQ8 (Page58 has this circuit)
[P33/P34/P36/P37] Exchange FBCWDQS* with FBCRDQS*
[58 -- H/W Thermal Protect] Modify HW protect circuit follow
"System Protection Shutdown Funciton(Tentative)-100730"
[06 -- SNB (POWER)] Add R155/R156 follow Intel PDDG
08/21
[70 -- OVP protection]Move PQ19/PR11/PR8 to DB
[59 -- MB to DB Conn] Rearrange CN37 pin define
08/23
[69 -- Others power plane] Change PR5/PR17/PR22 from 300K to 100K
[59 -- MB to DB Conn.] Update CN9 pin define
[59 -- MB to DB Conn] Rearrange CN37 pin define for layout request
08/24
[P27/P58] Delete ATI_SCL/ATI_SDA. Delete R548/R547/R545/R544
[11 -- PCH (PCI-E,SMBUS,CLK)] Add R157/Q28 follow FAE suggest (leakage protection solution)
[59 -- MB to DB Conn] Rearrange CN37 pin define for layout request
[59 -- MB to DB Conn] Reserve D26 for OVP
[66 -- CPU Power_VHCORE] Change PR290 to 9.31K. Change PR887 to 8.45K. Change PR292 to 43.2K
[69 -- Others power plane] Change PR28/PR29/PR36/PR37/PR63/PR42 to 150K
[70 -- OVP protection] Add PR174
[59 -- MB to DB Conn] Change CN35/CN37 to FOX_GB5SH500-1200-7H
[27 -- ATI VGA (I/O) 3/8] Change Q78 pin 1 to HW_THRMAL_SD#_ATI

08/25
[45 -- Debug Port] Change CN6 to P-TWO_196061-12021-3
[48 -- SATA ODD] Change CN14 to 196061-18041-3
[49 -- Camera] Add U26 co-lay with U24
[P33/P34/P35]Change NP_* to WS_*. Add SM_* parts
[68 -- VGA Power(ATI_VDD)] Modify AT_VDD control circuit
[68 -- VGA Power(ATI_VDD)] Add PR118 co-lay with PR113.Add PR181 co-lay with PR127
[43 -- EC + SPI ROM] Change R134/R133 to 3.9K_J
P.52 {USB3.0} Chenag the R22,R23,R59,R64,R83,R76 for layout space.

08/26
[58 -- H/W Thermal Protect] Change R532/R551 to 0402 size
[43 -- EC + SPI ROM] Change R66 to 0402 SIZE
[43 -- USB 3.0] Dummy U128/C460
[59 -- MB to DB Conn.] Change U20 to TPS2553DBVR-1.
[61-- Identify IC] Change PU22 to R5G05000N751NF
[45 -- Debug Port] Change CN6 to P-TWO_196061-12041-3
[58 -- H/W Thermal Protect] Add R591/R592/C533/C532

08/27
[27 -- ATI VGA (I/O) 3/8] Mount R6036 for GEN2
[41 -- Inverter] Delete J1/J2
[26 -- ATI VGA (Strap) 2/8] Dummy R6006/R6007
08/31
[68 -- VGA Power(ATI_VDD)] Change PR118 to 34.8K_F

DVT

09/01
[50 -- Status LED] Change R681/R682 pull high to +3VALW (For current leakage)
[68 -- VGA Power(ATI_VDD)] Change PR133/PR134 to 0 ohm (Power request)
09/03
[59 -- MB to DB Conn.] Add TP252/TP253/TP254/TP256/TP258 for BFT use
[71 -- Hole & BOSS & AMI LABEL] Delete H9. Delete LABEL1 (DXF updated)

09/07
[68 -- VGA Power(ATI_VDD)] Change PQ23 to SI2304DDS-T1-GE3(Power request)
[67 -- VCCSA] Change PR41 to 249K_F(Power request)
[55 -- TFM] Move TFM to DB(design change)
[59 -- MB to DB Conn.] Add CN39 for TPM(design change)

09/08
[49 -- Camera] Delete TP174/TP175/TP176/TP177
[59 -- MB to DB Conn.] Delete TP252/TP253/TP254/TP256/TP258

09/09
[44 -- EC (GPIO Extend)] Delete R407 [Double pull high]

09/10
[27 -- ATI VGA (I/O) 3/8] Delete R71/R68/R74/R75/R7/L152/L153/C1028/C1020/C1019/
C1026/C1021/C1029 (They are for Robson GPU)

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09/11
[70 -- OVP protection] Change PR9 to 0402 size (cost down)
[69 -- Others power plane] Change PR132/PR128/PR194/PR211 to 0402 size (cost down)
09/14
[43 -- EC + SPI ROM] Change R134/R133 pin1 from +3VALW to +ECVCC(Change SMB pull high)
[51 -- USB 2.0] Change CN30/CN32 to FOX_UB111P3-CE4S6-7H (connector list updated)
09/16
[26 -- ATI VGA (Strap) 2/8] Mount R5822. Dummy R5823/Q76/Q77/C6153/R5826 follow AMD's suggestion
[43 -- EC + SPI ROM] Add C535, Change R134/R133 to 7.5K (Power request)
[51 -- USB 2.0] Add C536. Dummy U129/U130/C492/C464 (cost down)
[52 -- USB 3.0] Delete F1, change R242 to 0.1u (cost down)
[46 -- FAN] Delete R589/R584/R585. Change C424 to 1u. Move C424 to FAN CONN side (cost down)
[32 -- ATI VGA (GND) 8/8] Change Q190/Q191/Q192/Q193 to SSM3K310T (PUR issue)
[63 -- VTT&PCH Power(+1_05V)] Change PR166 to 10K (Power request)
[67 -- VCCSA] Change PR159 to 10K (Power request)
[68 -- VGA Power(ATI_VDD)] Change PR118 to 330K. Change PR181 to 37.4K (Power request)
[42 -- HDMI] Change CN27 to QJ11AHL-NMSA-7H (connector list updated)
09/17
[52 -- USB 3.0] Change C241 to 470p (cost down)
[46 -- FAN] CN25 change to ACES_50208-0040N-001 (connector list updated)
[49 -- Camera] CN15 change to ACES_50208-0040N-001 (connector list updated)
[59 -- MB to DB Conn.] CN35/CN37 change to KOTL_F22250-H12101 (connector list updated)
[26 -- ATI VGA (Strap) 2/8] Mount R5823/Q76/Q77/R5826 .Change R5826 to 0 ohm
09/20
[69 -- Others power plane] Change PQ10/PQ13/PQ20 to SSM3J15F,LF (Power request)
[43 -- EC + SPI ROM] Change Q14 to LTA043ZUB FS8(PUR issue)
09/23
[49 -- Camera] Add test point for BFT
[56 -- Bluetooth Connector] Add test point for BFT
09/24
[40 -- LVDS] CN26 change to ENTERY_0880K-F40N-00L (connector list updated)
[56 -- Bluetooth Connector] CN19 change to P-TWO_196061-08041-3 (connector list updated)
[41 -- Inverter] Change SW3 to DHNF-04F-T-Q-T/R (default OFF)
[44 -- EC (GPIO Extend)] Change SW4 to DHNF-04F-T-Q-T/R (default OFF)
[07 -- SNB (GRAPHICS POWER)] Change R380/R385 to 1K_F (MOR Q&A 100923)
[P33/P34/P36/P37] Change C4040/C4033/C4041/C4034/C1617/C1618/C1620/C1621 to 0.1u (MOR Q&A 100923)
[59 -- MB to DB Conn.] CN39 change to ACES_50006-02071-002 (connector list updated)
09/27
[47 -- SATA HDD] Change +12V_1 to +12V
[64 -- DDR3 Power(+1_5V/+0_75V)] Change +0_75VRUN circuit (power cost down)
[44 -- EC(GPIO Extend)] Restore R407 and make it as NC(MOR Q&A 100927)
[43 -- EC + SPI ROM] Delete R142/R406 (MOR Q&A 100927)
[53 -- Mini-PCIE Card (WLAN)] Delete R465/R469 (MOR Q&A 100927)
[56 -- Bluetooth Connector] Add C537 (MOR Q&A 100927)
09/28
[47 -- SATA HDD] D12 change to SSM34APT (Small package)
[48 -- SATA oDD] D13 change to SSM34APT (Small package)
[20 -- DDRIII MD 1/5] U13 change to S-24C02CI-J8T1U
[32 -- ATI VGA (GND) 8/8] Q194 change to 2N7002ESPT (ESD)
[42 -- HDMI] Change Q32 to 2N7002ESPT (ESD)
[43 -- EC + SPI ROM] Change Q11 to 2N7002ESPT(ESD)
[44 -- EC (GPIO Extend)] Change Q19 to 2N7002ESPT(ESD)
[58 -- H/W Thermal Protect] Change Q8 to 2N7002ESPT(ESD)
[59 -- MB to DB Conn.] Change Q13 to 2N7002ESPT(ESD)
[64 -- DDR3 Power(+1_5V/+0_75V)] Change PQ21 to 2N7002ESPT (ESD)
[68 -- VGA Power(ATI_VDD)] Change PQ34/PQ37 to 2N7002ESPT(ESD)
[69 -- Others power plane] Change PQ17 to 2N7002ESPT(ESD)
[70 -- OVP protection] Change PQ9 to 2N7002ESPT(ESD)
09/29
[32 -- ATI VGA (GND) 8/8] Change R927/R929 pull high power to +5VRUN (AMD updated)
[43 -- EC + SPI ROM] Change Q14 to LTA043ZUBFS8TL
Change PR343/PR196/PR135/PR160/PR230 to 10k (power request)
09/29
P.19 [SO-DIMM] Add R6033,R6034 for DDR power for Intel request.
10/07
[59 -- MB to DB Conn.] Change CN9 to ENTERY_1001K-F80E-01L(connector list updated)
[59 -- MB to DB Conn.] Change CN9 pin define for 2L FPC
[64 -- DDR3 Power(+1_5V/+0_75V)] Add PQ472 and PR89 follow power request
[66 -- CPU Power_VHCORE] Add IMPV_VR_ON control circuit (Add PR739 PQ471 PC570 to control DB1_CORE)
Add change NTC circuit(Add PR740 and PR741 from PROCHOT#_R to NTC resistors)
Change VT1317 AVDD and AGND GND

10/07
[46 -- FAN] Change CN25 to ACES_50208-00401-001 (connector list updated)
[49 -- Camera] Change CN15 to ACES_50208-00401-001 (connector list updated)
[57 -- G sensor] Change R6021 to GP20 (Cost down)
10/08
[43 -- EC + SPI ROM] Dummy R412 and stuff R430, add TP254 (MOR request for JIG)
[50 -- Status LED] Change power of Q66/Q67/Q68 to +3VALW (MOR request for .leakage issue)
[27 -- ATI VGA (I/O) 3/8] Add back R6036 (GPIO_2: Pull-down for PCIe Gen1, Pull-high for PCIe Gen2 and depended on platform setting.)
[26 -- ATI VGA (Strap) 2/8] Add R6017 (Reserve GPIO_[0:1] strap and NC as default)
[12 -- PCH (DMI,FDI,GPIO)] Change R900 to 2.2K (NPIT check list)
[43 -- EC + SPI ROM] Delete R411 (Double pull high with R530)
[15 -- PCH (GPIO,VSS_NCTF,RSVD)] Mount R261 (Checklist V1.2 P80)
[16 -- PCH (POWER) 1/2] Dummy C419 (Only 0.1u is required-- NPIT PDDG V1.5 P154)
[16 -- PCH (POWER) 1/2] Change L17 to R65 0 ohm (NPIT PDDG V1.5 P154)
[13 -- PCH (LVDS,DDI)] Mount R228 and dummy R240 (NPIT-- Check ListV1.2 Page 63)
[13 -- PCH (LVDS,DDI)] Dummy R220/R222 (NPIT-- Design Guide V1.5 Page195)
[10 -- PCH (HDA,JTAG,SAT)] Delete R94 (Double pull high with R683)
10/10
[51 -- USB 2.0] Change C243/C841 to 6.3V for cost down
[20 -- DDRIII MD 1/5] Dummy U13/C104 for cost down
10/11
[48 -- SATA ODD] Reverse CN14 pin define for FFC use
[59 -- MB to DB Conn.] R87 change to 232K_F (MAX is 232K in datasheet)
[10 -- PCH (HDA,JTAG,SAT)] Add C231 follow EMI request
[52 -- USB 3.0] Add C538 follow EMI request
[64 -- DDR3 Power(+1_5V/+0_75V)] Mount ER43/EC20 follow EMI request
[66 -- CPU Power_VHCORE] Mount ER45/EC40/ER46/EC42 follow EMI request
[59 -- MB to DB Conn.] Add JP2 for power on use
10/12
[64 -- DDR3 Power(+1_5V/+0_75V)] Change PR735 to 39k,change PR736 to 38.3K (Power request)
[68 -- VGA Power(ATI_VDD)] Add PR214 (Power request)
[62 -- SYS Power (+3_3V/+5V)] Delete TP239/TP240/TP244/TP245 (Power request)
[17 -- PCH (POWER) 2/2] Change C197 to 10uF for CRT display noise issue
[43 -- EC + SPI ROM] Change C307/C308 to 33p follow SI test result
[66 -- CPU Power_VHCORE] Change PR741/PR740 to 56K and mount them
[57 -- G sensor] Add R6021 back follow MOR request
10/13
[71 -- Hole & BOSS] Change BOSS6/BOSS7 to F40M20-501028D4BM (Thermal request)
[56 -- Bluetooth Connector] Change CN19 to P-TWO_196061-10041-3 (Power ripple issue)
10/14
[17 -- PCH (POWER) 2/2] Change L57 to 0 ohm (NPIT suggestion)
[48 -- SATA ODD] Change power circuit for short test fail issue
[47 -- SATA HDD] Change power circuit for short test fail issue
[10 -- PCH (HDA,JTAG,SAT)] Change C115/C117 to 12p for SI crystal fail issue
[43 -- EC + SPI ROM] U16 pin E12 change to PM_SLF_S5# (MOR request GPIO table updated)
[43 -- EC + SPI ROM] U16 pin K9 change to PWRBTN# (MOR request GPIO table updated)
[43 -- EC + SPI ROM] U16 pin E9 change to KS016 (MOR request GPIO table updated)
[43 -- EC + SPI ROM] U16 pin E7 change to KS017 (MOR request GPIO table updated)
[44 -- EC (GPIO Extend)] U17 pin 14 change to MSK_FPBACK# (MOR request GPIO table updated)
[59 -- MB to DB Conn.] Change CN35 pin 9 to KS016(MOR request GPIO table updated)
[59 -- MB to DB Conn.] Change CN35 pin 4 to KS017(MOR request GPIO table updated)
[14 -- PCH (PCI,USB,NVRAM)] Add R277 for DEV_PRS_C
[15 -- PCH (GPIO,VSS_NCTF,RSVD)]Change U4 pin C40 to DEV_PRS_C(MOR request for Future chassis presence)
[59 -- MB to DB Conn.] Add R307/Q30 for +3V_FP discharge(For FP can not detect issue)
10/15
[59 -- MB to DB Conn.] Add F9 (For overload test fail issue)
[10 -- PCH (HDA,JTAG,SAT)] Add R136 follow intel DG1.5
[10 -- PCH (HDA,JTAG,SAT)] Change R117 to 1K follow intel DG1.5
[15 -- PCH (GPIO,VSS_NCTF,RSVD)] Delete R259 (GPIO table says it be float)
[59 -- MB to DB Conn.] Reserve R142/R144 for new keyboard
[65 -- SYS Power(+1_8V)] Change 1.8V power IC (Power request)
[14 -- PCH (PCI,USB,NVRAM)] Delete net DIMM_ALERT# (MOR request for EXTTS signal)
[59 -- MB to DB Conn.] Connect CN39 NC pin to GND (EMI request)
[19 -- DDRIII(SO-DIMM_0)]Change DDR CONN footprint to FOXCONN_AS0A626_JER6_4H_V030 (L6 EE request)
[39 -- CRT] Change CRT CONN footprint to FOXCONN_DZ11A91_MB1SD_9H_V030 (L6 EE request)
[56 -- Bluetooth Connector] Change CN19 back to P-TWO_196061-08041-3(MOR request)
[69 -- Others power plane] PC6 change to 0603 size (Power request)
10/18
[68 -- VGA Power(ATI_VDD)] Change PR 113 to 154K,change PR127 to 43K (For XTX_GPU)

10/18
[11 -- PCH (PCI-E,SMBUS,CLK)] Change Y2 to FOX_7A25000058 and change C135/C136 to 27P
(For SI test fail issue)
[69 -- Others power plane] Add R308/Q37 for leakage issue follow MOR suggestion
[43 -- EC + SPI ROM] Change R6032 to 12K_F follow MOR request of Q_A
[69 -- Others power plane]Add discharge circuit for +3VRUN/+3VSUS/+5VSUS/+5VSRM follow power request
[69 -- Others power plane] Set discharge circuit as NC
[39 -- CRT] Combine CRT bridge and damping resistor together :
Delete R230/R231 and change R908/R909 to 33_Ω (Cost down and save layout space)
[43 -- EC + SPI ROM] Add Q508/R465 for leakage issue on ADC power of EC (MOR suggestion)

10/19
[13 -- PCH (LVDS,DDI)] Dummy Q22 follow MOR suggestion
[59 -- MB to DB Conn.] Q30/R307 add 'FP_' prefix
[69 -- Others power plane] Add PU21/U131 to meet EC VCI rise and fall time spec ,and default as NC
(Follow MOR suggestion)
[52 -- USB 3.0] Add F1 back for USB logo requirement

10/22
[68 -- VGA Power(ATI_VDD)] PR214 add prefix SM_ follow POWER request

10/26
[65 -- SYS Power(+1_8V)] Change PQ464 to 17-2N7002E-SP00 (For PUR issue) -- ECR
[69 -- Others power plane] Dummy PQ19/PR35/PQ8/PQ5/PQ7 follow pwr request -- ECR
[69 -- Others power plane] Mount PU21/U131/Q38/Q39/Q40/Q41/R309/R312/R313/R314 pwr request -- ECR
[69 -- Others power plane] PR30 change to 2.8K pwr request -- ECR
[69 -- Others power plane] PC6 change to 4.7Ω pwr request -- ECR
[64 -- DDR3 Power(+1_5V/+0_75V)] Change PU17 to G2992FIU pwr request -- ECR
[66 -- CPU Power_VHOCORE] Change PR290 to 8.87K pwr request -- ECR
[63 -- VTT&PCH Power(+1_05V)] Change PR184 to 1R-0004422-B200 pwr request -- ECR
[63 -- VTT&PCH Power(+1_05V)] Change PR180 to 1R-0003832-B200 pwr request -- ECR
[69 -- Others power plane] Change PR33 to 560K pwr request -- ECR
[58 -- H/W Thermal Protect] Change R531 to 21K (HW shut down setting to 91.5°C) -- ECR
[58 -- H/W Thermal Protect] Change R549 to 18.2K (HW shut down setting to 95.5°C) -- ECR

10/27
[69 -- Others power plane] Change PR5 to 470K pwr request -- ECR
[39 -- CRT] Change R574/R576 to 4.75K for E010 CRT fail issue -- ECR
[61-- Identify IC] Change PU22 to R5G05000N753NF pwr request -- ECR

10/28
[14 -- PCH (PCI,USB,NVRAM)] R104 add prefix WS_, R105 add prefix SM_
[58 -- H/W Thermal Protect] Dummy Q10 (There is risk to wrong action)
[43 -- EC + SPI ROM] Dummy R112, mount R107(MOR request) -- ECR
[59 -- MB to DB Conn.] Change R87 to 226K_F (MOR request) --ECR

10/29
[41 -- Inverter] Change panel ID table follow MOR suggestion

11/01
[02 -- Block Diagram] Update block for audio codec change to ALC275 and TPM move to DB
[65 -- SYS Power(+1_8V)] Change PQ464 to 2N7002W (EEC-V030-00287-H)
[66 -- CPU Power_VHOCORE] Change PL10 to 1L-D1205AS-H100 (HF, DVT EEC-V030-00287-H)
[69 -- Others power plane]Change PR42 to 47K_Ω (DVT EEC-V030-00287-H)

PVT

Base on 'V030 DVT MB SCHEMATICS_1101_1402_ECR.DSN'

11/01
[62~68] Short open jump
[65 -- SYS Power(+1_8V)] Change PQ464 to 2N7002ESPT (ESD protection)

11/02
[66 -- CPU Power_VHOCORE] Change PU10 to VT1316MAFQX-001 (Vendor update component)

11/08
[02 -- Block Diagram] Update block diagram

11/10
[52 -- USB 3.0] Change U51 from μPD720200AF1-DAK-A to μPD720200AF1-DAP-A (Vendor PN&Vendor updated)

11/16
[40 -- LVDS] Set CN26 pin4/7/34/35/36/37/40 as NC

11/17
[51 -- USB 2.0] Delete TP178/TP179/TP180/TP181 (L6 TE feedback, can be delete)
[59 -- MB to DB Conn.] Add TP198/TP199/TP200 follow L6TE request

11/18
[47 -- SATA HDD] Change CN13 to ENTERY_1001K-F60E-05L (Connector list updated)
[64 -- DDR3 Power(+1_5V/+0_75V)] PU17 PIN6 add PC8 (Power request)
[66 -- CPU Power_VHOCORE]Change PU11/PU12/PU7 to VT1317SFCX-001 (Vendor PN updated)
[71 -- Hole & BOSS] Change BOSS1 to 1M-1A40M20-3001 (Connector list updated)

11/19
[43 -- EC + SPI ROM] Change R442/R448 pin1 to +3VALW from +ECVCC (Q&A sheet)
[67 -- VCCSA] Change PU13 to VT355FCX-ADJ (Vendor PN updated)

11/22
[32 -- ATI VGA (GND) 8/8] Mount R941 (For PX3 mode)
[32 -- ATI VGA (GND) 8/8] Dummy Q190, Q191, Q192, Q193, Q194, Q496, U19, C246, R926, R927 and R929

11/23
[66 -- CPU Power_VHOCORE] Change PR82/PR85/PR91/PR94 to 6.8K from 4.3K (Power request)
[59 -- MB to DB Conn.] Delete TP182

11/24
[06 -- SNB (POWER)] Dummy R57 (Pull high at device side)
[66 -- CPU Power_VHOCORE] Mount PR68 (Pull high at device side)
[66 -- CPU Power_VHOCORE] Dummy PR739/PC570/PQ471
[06 -- SNB (POWER)] Change R52/R54/R58 to close gap
[07 -- SNB (GRAPHICS POWER)] Change R67/R102 to close gap
[10 -- PCH (HDA,JTAG,SAT)] Change R95/R332 to close gap
[11 -- PCH (PCI-E,SMBUS,CLK)] Change R174 to close gap
[12 -- PCH (DMI,FDI,GPIO)] Change R205 to close gap
[15 -- PCH (GPIO,VSS_NCTF,RSVD)] Change R327/R336 to close gap
[16 -- PCH (POWER) 1/2] Change R323/R328/R331/R65/R330/R319/R321/R322 to close gap
[17 -- PCH (POWER) 2/2] Change R338 to close gap
[27 -- ATI VGA (I/O) 3/8] Change R6014 to close gap
[30 -- ATI VGA (Power) 6/8] Change R6018 to close gap
[39 -- CRT] Change R580/R906/R907/R910/R911/R912 to close gap
[43 -- EC + SPI ROM] Change R887 to close gap
[49 -- Camera] Change R26/R27 to close gap
[51 -- USB 2.0] Change R8/R16/R20/R21 to close gap
[52 -- USB 3.0] Change R763/R22/R23/R59/R64/R83/R76 to close gap
[53 -- Mini-PCIE Card (WLAN)] Change R886/R78/R24/R25 to close gap
[56 -- Bluetooth Connector] Change R28/R30 to close gap
[57 -- G sensor] Change R6021 to close gap
[58 -- H/W Thermal Protect] Change R537/R591/R592 to close gap
[59 -- MB to DB Conn.] Change R109 to close gap

11/25
[32 -- ATI VGA (GND) 8/8] Dummy R935 for follow NDA_1.02
[62 -- SYS Power (+3_3V/+5V)] Change PR122 to 2.2_Ω (Power request)
[62 -- SYS Power (+3_3V/+5V)] Change PR341/PR198 to close gap
[63 -- VTT&PCH Power(+1_05V)] Change PR177 to close gap
[64 -- DDR3 Power(+1_5V/+0_75V)] Change PR105/PR106 to close gap
[65 -- SYS Power(+1_8V)] Change PR313 to close gap
[67 -- VCCSA] Change PR158/PR155 to close gap
[68 -- VGA Power(ATI_VDD)] Change PR138 to close gap
[69 -- Others power plane] Change PR46/PR13 to close gap
[70 -- OVP protection] Change PR38/PR7 to close gap

11/26
[39 -- CRT] Dummy C639/C638/C467/C470 (DDC rise time fail issue)
[39 -- CRT] Change R471/R472 to 3.3K (SI DDC fail issue)
[43 -- EC + SPI ROM] RSM_ON_EC add 100k pull low (SI PWRBTN# pulse issue)
[45 -- Debug Port] Change CN7 Pin17 to PWRSW#_DB (MOR QA request)
[15 -- PCH (GPIO,VSS_NCTF,RSVD)] Update MEM PRS table

11/29
[69 -- Others power plane] Change PU3 power supply to +5VALW (Power request)
[69 -- Others power plane] Change PR44 TO 200K (Power request)
[47 -- SATA HDD] Add C232 (SSD power pk-pk ripple test fail)
[59 -- MB to DB Conn.] Add R52 (reserve for over load test fail)
[59 -- MB to DB Conn.] Change CN9 PIN 39 to +3VALW from AC_OFF_EC#(Power request)
[39 -- CRT] Add C639/C638 back
[39 -- CRT] Change R472/R471 back to 3.9K
[14 -- PCH (PCI,USB,NVRAM)] Add C826 (EMC request)
[48 -- SATA ODD] Mount D13 and change to SL22 (EMC request)
[43 -- EC + SPI ROM] R904 change to 10K follow T8 circuit solution (NPIT)
[40 -- LVDS] Change CN26 Pin 36/37/40 to LCDVCC from NC (Reserve for 15'')
[40 -- LVDS] Change CN26 Pin 34 to GND (EMI request)
[43 -- EC + SPI ROM] Reserve R145 for PECI undershoot issue

11/30
[43 -- EC + SPI ROM] Add 100K pull down resistor R482

12/01
[51 -- USB 2.0] Mount U129/U130/C464/C492 (MOR request for ESD)

12/02
[62 -- SYS Power (+3_3V/+5V)] Dummy PR233, stuff PR232 (Power request)
[43 -- EC + SPI ROM] Add R484/R485/R486/R487 follow MOR request
[43 -- EC + SPI ROM] Add close gap and resistor in SMB follow MOR request
[58 -- H/W Thermal Protect] Change R531 to 29.4K,
change R549 to 21K (Thermal request)

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12/02
[59 -- MB to DB Conn.] Delete R52 (Move to DOCKING DB)
[59 -- MB to DB Conn.] Add R1101/R1102/R1103/R1104/R1105/R1106 (For over load test fail issue ,shall change to fuse)
[47 -- SATA HDD] Add R1107 (For over load test fail issue ,shall change to fuse)
[53 -- Mini-PCIE Card (WLAN)] Add R1108 (For over load test fail issue ,shall change to fuse)
12/03
[27 -- ATI VGA (I/O) 3/8] Add Q20/R6037 (+3V3_DELAY leakage issue)
[11 -- PCH (PCI-E,SMBUS,CLK)] Reserve R146 follow NPIT suggestion
[47 -- SATA HDD] Delete R1107 (Placement difficulty)
[59 -- MB to DB Conn.] R1101 co-lay with F2,R1102 co-lay with F3,R1103 co-lay with F10,R1104 co-lay with F11
[59 -- MB to DB Conn.] R1105 co-lay with F14,R1106 co-lay with F15
[53 -- Mini-PCIE Card (WLAN)] R1108 co-lay with F13
MP
12/24
[10 -- PCH] For PVT hung up 767C issue change C121 from 2.2uF to 10uF
[43 -- EC+SPI ROM] For ALS follow MOR request R6032 changefrom 120Kohm to 110Kohm
[43 -- EC+SPI ROM] change capcitor (C7368)value from 10uF to 2.2uF for ALS follow MOR request
[43 -- EC GPIO Extend] For BT2_PRS# Issue R436 ,R407change fromNC to munt,R441 change from munt to NC
[53 -- Wlan] Due to concern of fuse voltage drop is larger than resistor, need delete F13 and add R1108
[68 -- VGA Power] Our current AT_VDD is not meet AMD the min spec Change PR118 From 1R-0000334-F200 to 1R-0000474-J200
12/25
[43 -- EC+SPI ROM] For MOR request change R484~R487 from 0ohm(1R-0000000-J200) to 22ohm(1R-0000220-J200)
12/27
[44 -- EC GPIO Expended] For WWAN ID Issue change RP44 from 1R-1020103-J100 to 1R-1020102-JX02
12/27(2)
[68 -- VGA Power] For V030 MP PR118 change from 5%(1R-0000474-J200) to 0.5%(1R-0004703-D200)
[16 -- PCH(Power)] For quality issue 1C-33T0227-M102 forbit to use C148,C149 change to 1C-33T0227-M102
[27 -- ATI VGA(IO)] For description issue R6037 change to 1R-0000103-J200
[77 -- 2nd source] For quality issue 1C-33R0157-M101 forbit to use delete CAP7_1,CAP16_1,CAP21_1
12/28
[10 -- PCH(HDA,JTAG)] For PVT hung up 767C issue add C233 10uF,then add C234 (1C-2B30225-K101)
2011/01/04
[45 -- Debug port] For MP, change R123 to stuff and U35/R121/C891/CN6 to NC
[43 -- EC,SPI ROM] Y4 Change 1F-X32K768-2006 to 1F-X32K768-200F on MP.Because 1F-X32K768-2006 EOL
[10 -- PCH] Y12 Change 1F-X32K768-2006 to 1F-X32K768-200F on MP.Because 1F-X32K768-2006 EOL
[26 -- ATI VGA(Strap)] For +3VRUN voltage drop issue NPIT suggest C6153 change to mount
[48 -- SATA ODD] For EMI request delete C830,C829(1C-2N20330-J000) then reserve VR1,VR2(19-MLVS060-5000)
2011/01/05
[46 -- FAN] For SI CRT leakage issue add 47Kohm resistor R544(1R-0000473-J200)
[17 -- PCH(Power)] For SI system voltage issue delete L54 (1L-BBCMS45-1600)Net name +V1.05S_VCC_EXP change to +1_05V_VTT
2011/01/07
[67 -- VCCSA] Change PU13 footprint to(bga_15p_20_76x105_V030)
2011/01/20
[51 -- USB 2.0] Update U129/U120 vendor PN AZC002-02N.R7G ECR06546
[66 -- CPU Power_VHCORE] Change PU10 from 15-VT1316M-0001 to 15-VT1316M-0002 (other project have shutdown issue by VOLTERRA IC(15-VT1316M-0001))